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"HTS Josephson Technology on Silicon with Application to High Speed Microelectronics"

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13. ABSTRACT (Maximum 200 words)

Superconducting electronics have long been regarded as having the potential for superior switching speeds and reduced power consumption compared to semiconducting devices. High temperature superconducting materials, such as $YBa_2Cu_3O_7$, present many new opportunities. Because many targeted applications of superconducting electronics rely on the high switching speeds attainable by Josephson junctions, however, rf properties have played a significant role in the search for practical substrates. The overall goal of this Phase II STTR program, a collaboration between Advanced Fuel Research, Inc. and the State University of New York at Stony Brook, was to develop an ultrahigh-speed superconducting electronics technology using electron beam modified high temperature superconducting Josephson junctions on silicon and other rf compatible substrates. Considerable success was achieved towards the development of a compliant substrate technology that could potentially enable growth of low-stress $YBa_2Cu_3O_7$ on silicon. Also, a model was developed describing the formation and degradation properties of electron beam modified junctions, thus serving as a reliable basis for the description of the junctions and allowing for better control of the process and better reproducibility of the devices. Unfortunately, however, the program was unsuccessful in demonstrating working junctions and junction-based devices due to equipment problems and loss of key technical personnel.

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1. Executive Summary

Superconducting electronics have long been regarded as having the potential for superior switching speeds and reduced power consumption compared to semiconducting device families, however, the requirement for refrigeration to temperatures near 4.2 K has been a major stumbling block to the commercialization of low T_c superconducting logic. High temperature superconducting (HTS) materials, such as $YBa_2Cu_3O_7$ (YBCO) present new opportunities for superconducting electronics. Because many targeted applications of superconducting electronics rely on the high switching speeds attainable by Josephson junctions, however, rf properties have played a significant role in the search for practical substrates. Silicon, quartz, and glass substrates are attractive substrates for HTS device technology due to, 1) large size, availability and low cost, 2) superior dielectric, thermal conduction, and strength properties compared to traditional substrate materials, 3) compatibility with both VLSI silicon and HTS materials technologies, and 4) extensive preexisting technology base. Silicon-on-sapphire offers many of these benefits as well.

The overall goal of the Phase II program was to develop an ultrahigh-speed superconducting electronics technology using HTS Josephson junctions and thin films on silicon and other rf compatible substrates. The Phase II program objectives were to, 1) optimize the junction fabrication process for uniformity, controllability, and thermal stability, 2) develop a new class of "compliant substrates" for films with improved rf properties, reduced stress, and multilayer capability, 3) integrate the e-beam modified Josephson junctions and passive superconducting devices on silicon and compliant substrates, and 4) demonstrate working circuits on practical low loss substrates with non-trivial numbers of junctions.

The Phase II program was led by Advanced Fuel Research, Inc. (AFR), who were primarily involved in the thin film materials development and fabrication of the project. Subcontractors included the State University of New York (SUNY) at Stony Brook, who were responsible for e-beam modified junction fabrication and On-Line Technologies, Inc. (On-Line), who consulted on the development of the compliant substrate technology. Conductus was also involved with the anticipated role of scaling the technology to larger wafer sizes.

Unfortunately, the main goal of developing a fast superconducting technology using HTS Josephson junctions on silicon could not be completed. SUNY experienced equipment and personnel problems, which could not be resolved, and were thus unable to fabricate the junctions required for this project. For this reason, the funding allocated to this project by the Navy was not entirely spent. However, various technical successes were achieved including the following:

- The YBCO thin film deposition facility was modified to allow improved film quality and uniformity on larger substrates. High quality YBCO films were grown on both silicon and SOS substrates. The use of a double buffer layer was observed to improve the film structure.
- A theoretical model was developed which describes the formation and degradation properties of the e-beam junctions and can serve as a reliable basis for the description of e-beam junctions. It also accounts for the influence of various microscopic parameters on the final properties of the junctions, thus allowing for better control of the technological process and, as a result, enabling better reproducibility and predictability of the devices.
- Studies were conducted on the stability of e-beam irradiated YBCO films (on $LaAlO_3$ substrates). Some important insights into the annealing kinetics involved were obtained.
- Considerable success towards developing a compliant substrate technology was achieved, which potentially could enable crack-free growth of high quality YBCO, > 70 nm thick, on silicon. The work demonstrated that, employing appropriate thin film buffer materials, high quality HTS films could be grown on CaF_2 surfaces. In addition, a promising compliant substrate methodology utilizing CaF_2 thin film buffers was devised.

"HTS Josephson Technology on Silicon with Application to High Speed Microelectronics"

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2. Phase II Proposal

2.a. Introduction and Background

Manufacturable High Temperature Superconducting Digital Electronics

Superconducting electronics have long been regarded as having the potential for superior switching speeds and reduced power consumption compared to semiconducting device families, however, the requirement for refrigeration to temperatures near 4.2 K has been a major stumbling block to the commercialization of low T_c superconducting logic. High temperature superconducting (HTS) materials present new opportunities for superconducting electronics.

At present there are very few Josephson HTS technologies which can be considered for applications requiring a non-trivial number of high quality junctions. Among these are SNS junctions; where N may be a noble metal [1] or a conductor compatible with HTS materials[2], bi-epitaxial junctions [3], and e-beam written junctions [4]. It is fair to say that none of the existing HTS Josephson technologies have fully matured, and much additional work is required to make them useful in applications. Because many targeted applications of superconducting electronics rely on the high switching speeds attainable by Josephson junctions, rf properties have played a significant role in the search for practical substrates. Silicon, quartz, sapphire and glass substrates are attractive substrates for HTS device technology due to:

- Large size availability and low cost
- Superior dielectric, thermal conduction, and strength properties compared to MgO or the perovskite related substrate materials [5].
- Compatibility with both VLSI silicon and HTS materials technologies through various wafer bonding or ion-implantation fabrication procedures.
- Extensive preexisting technology base.

HTS Digital Josephson Technology for Silicon and Other rf Compatible Substrates

A method for growing epitaxial thin films of $Y_1Ba_2Cu_3O_7$ (YBCO) on silicon substrates and the demonstration of YBCO Josephson junctions on silicon during Phase I brought the possibilities of practical manufacturable, high performance superconducting electronics closer to reality. The adoption of silicon as a substrate material raises the tantalizing possibility of a monolithically integrated technology, combining the speed and power consumption of superconducting electronics with the tremendous benefits offered by modern VLSI silicon technology. In addition to novel hybrid applications involving integrated semiconducting and superconducting components, a Josephson technology fully compatible with silicon substrates would find broad acceptance for most of the classic applications of the Josephson effects [6] including Superconducting Quantum Interference Devices (SQUIDs), Josephson array oscillators, infrared detectors, Josephson mixers and heterodyne receivers, digital logic, A to D converters, and millimeter/submillimeter-wave spectrum analyzers.

Developments in wafer bonding and etchback raise the additional possibility of developing a YBCO technology for silicon, quartz or glass substrates with greatly reduced stress due to thermal expansion mismatch during growth and cooldown. Applying these techniques could greatly improve the performance of many rf components such as filters, delay lines and receivers as well as high-speed active Josephson components.

Summary of Phase I

Phase I was performed in three tasks with the following objectives:

Task 1 - Josephson Junction Fabrication and Testing: To verify the junction fabrication process on silicon substrates, and to produce a set of junctions for electrical and statistical testing.
Task 2. - RSFQ Logic Modeling and Design: To design and simulate RSFQ circuit elements that can be successfully fabricated and tested.
Task 3. - RSFQ Circuit fabrication and Testing: To fabricate working HTS RSFQ logic elements on silicon substrates.

The junction technology developed in Phase I was based on the electron beam modification technique. To summarize briefly, thin yttria stabilized zirconia (YSZ) buffered HTS films were deposited on silicon substrates, and patterned into narrow ~4 μm wide bridges. These bridges were then written over by a narrow (~5 nm width) electron beam of high energy. The electron beam has the effect of "damaging" the HTS material over a length comparable to the coherence length, forming a Josephson junction. The electron beam writing process is believed to be associated with the formation of displaced-oxygen/vacancy pairs in the crystal structure that locally disrupt the superconductivity. Although the quality of the junctions in the exploratory Phase I program was relatively good, several factors associated with the use of silicon as a substrate emerged as technical barriers.

HTS film thickness was identified as a particularly important factor. It is necessary to minimize parasitic inductance in order to achieve high quality HTS RSFQ circuits, and to do this thicker films are required. The maximum crack-free YBCO film thickness on YSZ-buffered silicon seems to be about 70 nm. The 25 nm films used in Phase I were adequate for forming good junctions, as determined by the measurements of Shapiro steps, and the magnetic modulation, but this is not good enough for complex circuits. To obtain the required thicker films, without cracking, we devised methods to use a compliant buffer layer on the silicon substrates. This buffer layer, of a plastically deformable glass, would relieve the stress due to differential thermal expansion between the silicon wafer and the YBCO, potentially allowing thick (>500 nm) crack-free YBCO films.

The Phase I program clearly demonstrated that it is possible to fabricate high quality YBCO Josephson junctions on silicon substrates, and that complex HTS devices can be fabricated. The highlights of the Phase I accomplishments include:

- Working Josephson junctions and SQUIDs have been fabricated on silicon substrates. The electrical properties are similar to those fabricated on more conventional substrates such as $LaAlO_3$.
- **A YBCO RSFQ RS flip flop with 14 junctions and I/O test structures was successfully designed, fabricated and tested.**
- The kinetic inductance and London penetration depth of the films on silicon have been determined from measurements of HTS SQUIDs on silicon.
- An approach to alleviating film stress due to thermal expansion coefficient mismatch has been outlined. The proposed solution involves fabricating a functionally graded buffer layer that flows plastically to relieve film stress while at the same time, allows nucleation and growth of heteroepitaxial films.
- A wafer bonding facility was constructed at AFR and utilized to demonstrate the successful bonding of silicon and BPSG coated wafers, a key step in the compliant substrate fabrication procedure.

2.b. Phase II Objectives and the Degree to Which They Were Met

The overall goal of the Phase II program was to develop an ultrahigh-speed superconducting electronics technology using HTS Josephson junctions and thin films on silicon and other rf compatible substrates. This was to be accomplished through the following tasks:

Task 1 - Junction Refinement - To improve the fabrication process for the e-beam Josephson junction technology.

The majority of this task was successfully completed. Highlights include:

- Various modifications to the PLD system were implemented to improve the YBCO film uniformity and to increase the deposition area.
- The use of a double buffer layer, CeO_2/YSZ to improve the epitaxy of the YBCO layer was investigated. Significant improvements in the YBCO film structure for films incorporating the additional CeO_2 buffer layer were observed.
- Growth of YBCO on SOS wafers was investigated. The SOS wafers could potentially support thicker YBCO films than Si due to the better match of thermal expansion coefficients. High quality, thicker films of YBCO (~160nm thick) were successfully grown on SOS.
- Some of AFR's technology for growing YBCO on Si was transferred to Conductus. The thinner films (~50nm) were comparable to films grown directly on YSZ substrates.
- To study the stability of the e-beam junctions at SUNY, samples of microbridges were prepared from films grown using conventional techniques. A complete set of resistivity, Hall, V (I) measurements was performed on these films and followed by annealing at different temperatures in He atmosphere.
- A theoretical model was developed which describes the formation and degradation properties of the e-beam junctions and can serve as a reliable basis for the description of e-beam junctions. It also accounts for the influence of various microscopic parameters on the final properties of the junctions, thus allowing for better control of the technological process and, as a result, enabling better reproducibility and predictability of the devices.

Task 2: Junction Stability through Improved Chemistry - To improve the thermal stability of the e-beam modified junctions.

This task was partially successful. Highlights include:

- SUNY studied the annealing kinetics (stability) of the e-beam-irradiated YBCO films on $LaAlO_3$ to serve as background measurements needed for the comparison with data on the stability of substituted YBCO films and films on Si substrates.
- The data on the time evolution of the critical temperature are well described by the so-called stretched exponential kinetics expression.
- The cooling-warming cycle increases the resistance of the film perhaps due to accumulation of some stresses in the film. Annealing of these stresses is characterized by its own kinetics that seems to be a simple exponential.

Task 3 - Device Integration - To develop the capability to integrate the junctions onto rf compatible substrates with wiring, groundplane and crossover structures.

This task resulted in considerable success towards developing a compliant substrate technology which potentially could enable crack-free growth of high quality YBCO, > 70 nm thick, on Si. Highlights include:

- The following three potential compliant substrate technologies were considered, 1) viscoelastic glass buffer layer, 2) CaF_2 buffer layer, and 3) film transfer (epitaxial liftoff). All three were determined to be promising methods, however, we focused on the CaF_2 buffer method because it was considered to be most suited to our capabilities.
- Initial work studied growth of YBCO on CaF_2 single crystal substrates. Success was achieved in demonstrating high quality, epitaxial growth of YBCO on (CeO_2)/YSZ buffered CaF_2.
- A thermal evaporation system was constructed to deposit CaF_2 thin films on Si. Good quality, epitaxial CaF_2 films grown on Si(100) were obtained with this system.
- Growth of epitaxial, superconducting YBCO, incorporating CeO_2/YSZ buffer layers on CaF_2-coated Si was successfully demonstrated. However, the YBCO films showed stress-related microcracks, which may have resulted because of CaO formation in the CaF_2 layers. To solve this problem, a plan was devised to add an oxygen diffusion barrier layer which would protect the CaF_2 layer and also support epitaxial growth of YBCO. Unfortunately, further work was discontinued due to problems at SUNY.

Task 4 - Task 4 -Film Characterization and Stress Analysis - To measure structure, morphology, stress and electrical properties of YBCO films and devices.

This task was completed as needed in support of Tasks 1, 2 and 3.

Task 5 - Demonstration Circuits (Stony Brook, AFR/On-Line) - To demonstrate working HTS electronic circuits on silicon, sapphire and compliant substrates.

Not completed due to equipment and personnel problems at SUNY.

Option Task 6 - Advanced Demonstration Circuits - To design, fabricate and test circuits comprised of multiple RSFQ elements and passive rf structures.

Not funded.

3. Detailed Results and Discussion

Task 1: Junction Refinement - To improve the fabrication process for the e-beam Josephson junction technology.

In the Phase I program, the junctions produced were not well controlled due to variations in the $YBa_2Cu_3O_7$ (YBCO) films and the processing parameters. The junctions were produced on small substrates (10 mm x 10 mm), which we believe contributed to variations in the film and junction properties across each chip. During Task 1 of this Phase II program, an important goal was to improve our pulsed laser deposition (PLD) facility to allow us to routinely grow high quality films on Si, and also to expand our deposition capabilities to allow high quality YBCO growth on silicon-on-sapphire (SOS). We also modified the system to enable deposition of YBCO on larger substrates (> 25 mm x 25 mm) for two reasons. First, more junctions could be produced per chip, thus allowing us to design and test more complicated structures. Second, larger substrates could be diced into several chips of similar properties, which would allow more controlled experiments on the junctions. Details on the facility modifications, YBCO/Si film growth and YBCO/SOS film growth are discussed in more detail below. In addition, some results for YBCO films grown at Conductus are presented.

During the initial period of the Phase II program in which AFR was improving the PLD facility and optimizing deposition conditions on Si and SOS substrates, SUNY concentrated on developing a deeper understanding of the physical mechanisms governing the process of e-beam junction fabrication. Through this effort, SUNY established factors determining junction quality, uniformity and reproducibility. Since YBCO films on Si or SOS were not yet available, SUNY conducted this initial research using films grown on $LaAlO_3$ substrates. Although some differences for films grown on Si could be expected, due to differences in microstructure, morphology and stress, the opinion was that the majority of the results and conclusions obtained from experimental data using YBCO/$LaAlO_3$ would be applicable to films grown on Si. These findings are also discussed below. Unfortunately, at the point during the program in which AFR began sending high quality films to SUNY for junction fabrication studies, SUNY experienced equipment and personnel problems which could not be resolved (See Task 5 for details), therefore, no junctions could be fabricated on Si or SOS for further study.

PLD Facility Improvements - Various modifications to our PLD system were implemented to improve the YBCO film uniformity and to increase the deposition area. First, we converted our single-axis mirror scanner to a two-axis system to increase the raster area on the film material targets. The new mirror scanning system, in addition to rastering in two directions, has a larger angular range and is operable at higher frequencies. Our translatable target holder was modified to support two-inch diameter targets, which was necessary to assure uniform coverage of the one-inch substrates. We also designed and constructed a larger, more robust substrate heater, capable of heating substrates up to one square inch. The heater incorporates two silicon carbide elements for radiative heating of both Si and SOS substrates and is capable of heating Si >1000 °C with ramp rates ~ 10 °C/second.

Our best films were produced as follows. The Si substrate is cleaned using various organic solvents (trichloroethylene, acetone, isopropanol and reagent alcohol), and the native oxide is then removed using the "spin-etch" technique [7]. The substrate is then loaded into our deposition chamber and the chamber is pumped down to base pressure (~ 5 x 10^{-6} Torr). The substrate is first heated to ~300 °C for about one hour and then quickly heated to 790 °C, at which point the deposition of theYSZ buffer layer (~50 nm thick) begins. Oxygen is *immediately* introduced into the chamber at a pressure of 0.4 mTorr. Following the YSZ deposition, the chamber pressure is raised to 200 mTorr O_2 and the substrate temperature is adjusted to 775 °C for YBCO deposition. Following the YBCO deposition, the chamber pressure is raised

to ~ 350 Torr O_2, and the substrate temperature is quickly lowered to ~500 °C where it is held for 15 minutes and then cooled to room temperature. Figure 1 presents the resistance vs temperature for a nominally 50 nm thick YBCO film grown on a 1 cm x 1 cm YSZ-buffered Si chip, deposited with the improved system. The zero resistance T_c is 87.5 K with a width (10 – 90%, ΔT_c) of < 1 K.

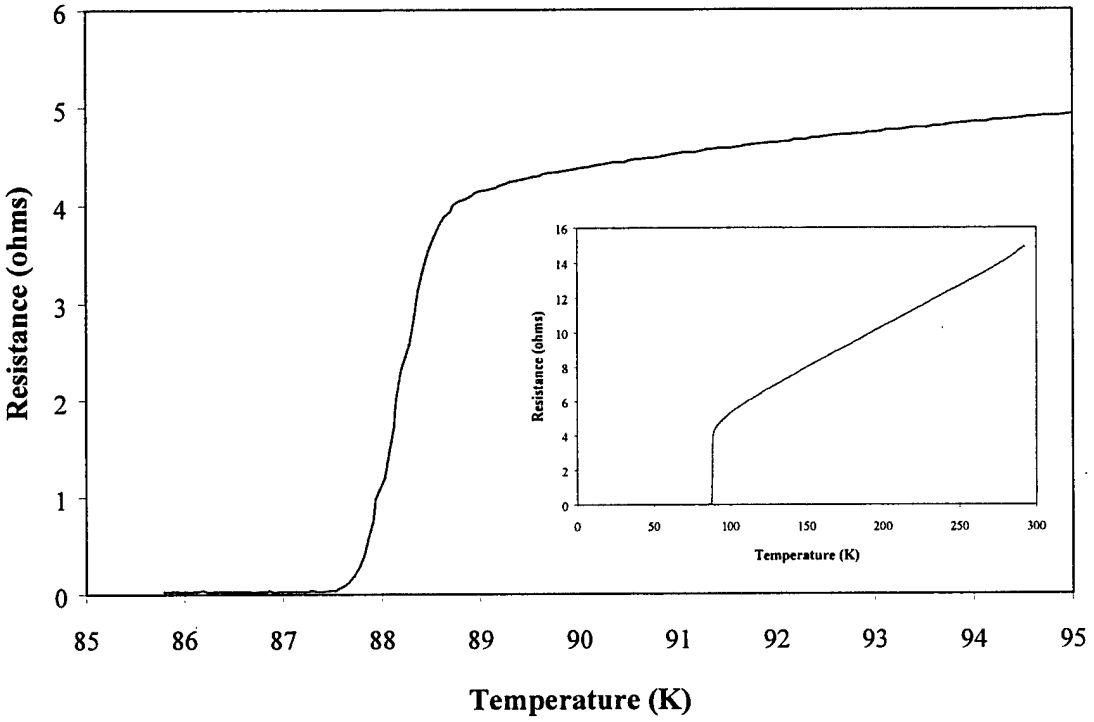

Figure 1. Resistance vs temperature for a typical 50 nm thick YBCO film grown on YSZ-buffered Si(100).

Across one-inch Si chips, we found the temperature uniformity to be better than ± 3 °C, determined using the handheld near-IR pyrometer. With this improved system, we found that YBCO films grown on the one-inch Si substrates were comparable to the films routinely grown on one-cm substrates, with T_c ~ 88 K and ΔT_c ~ 1 K. In addition, one representative film was sent to NIST for x-ray diffraction (XRD) analysis and determined to be c-axis oriented.

During the program we also investigated the use of a double buffer layer, CeO_2/YSZ, to improve the epitaxy of the YBCO layer - CeO_2 has a closer lattice match to YBCO (when rotated 45°). The CeO_2 film was grown immediately following the YSZ layer using essentially the same deposition conditions as for the YSZ (0.4 mTorr O_2, 800 °C). Although the R vs T measurements for films grown with and without the CeO_2 layer were similar, we observed significant improvements in the YBCO film structure, for films incorporating the additional CeO_2 buffer layer. Figure 2 depicts XRD patterns for the YBCO/CeO_2/YSZ/Si(100) sample. From the two-theta scan, the YBCO is shown to be c-axis oriented and both the CeO_2 and YSZ are well oriented (out of plane). The phi scan of the YBCO(103) peak confirms that the film is epitaxial and single domain, rotated 45° with respect to the underlayers and the Si substrate. In addition, the rocking curve full width at half maximum (FWHM) of the YBCO(005) peak (not shown), 0.48°, is narrower than our films grown with only the single YSZ buffer layer, indicating improved out of plane grain alignment.

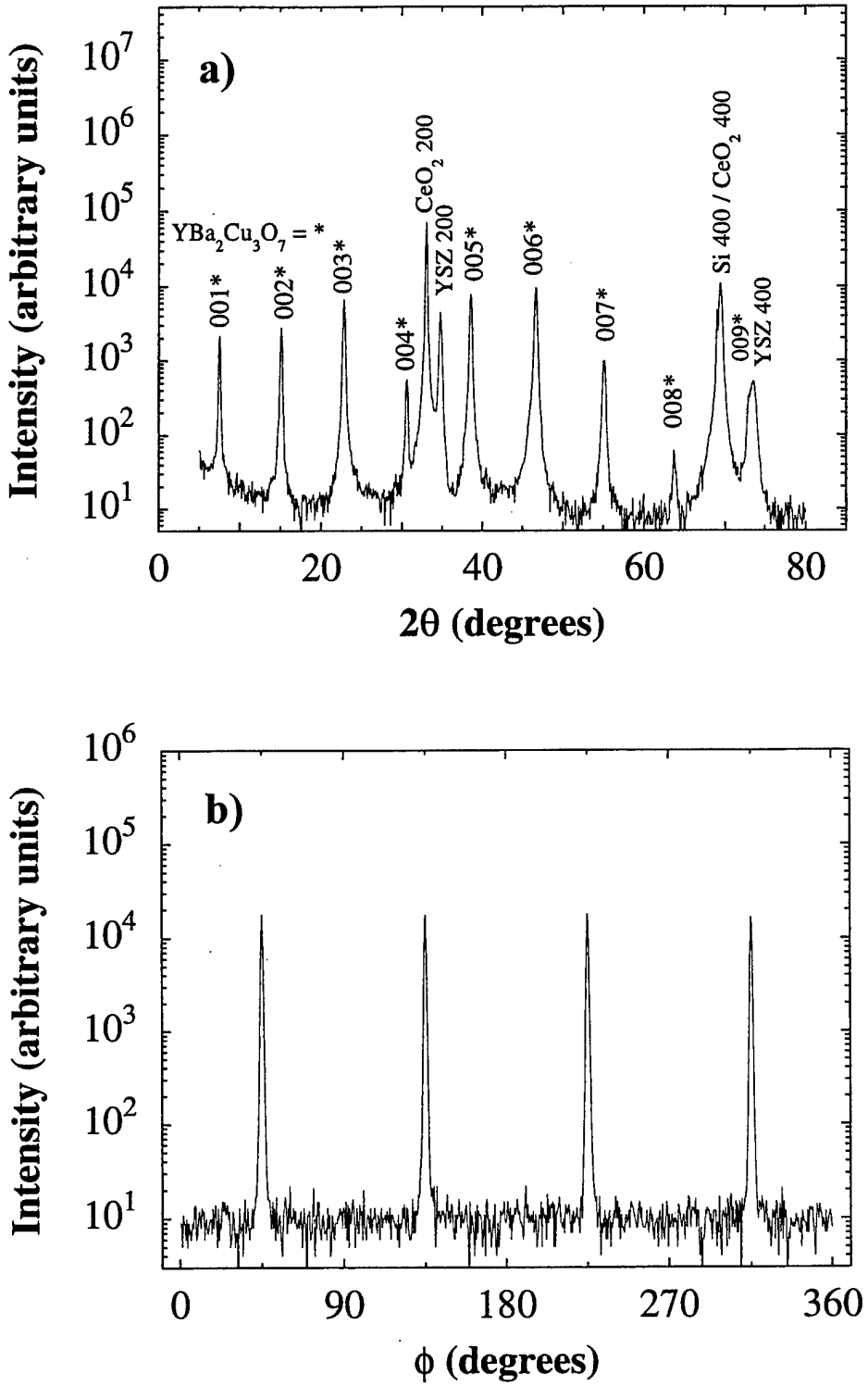

Figure 2. XRD patterns for a YBCO film grown on CeO_2/YSZ-buffered Si(100): a) two theta scan, b) phi scan of the YBCO(103) peak.

YBCO on Silicon-on-Sapphire – An important aspect of this program was to evaluate junction properties related to YBCO film thickness. In Phase I, parasitic inductance was identified as a critical parameter affecting the performance of HTS RFSQ devices. Our goal was to grow crack-free YBCO films (on Si) several times thicker than those grown in Phase I (~ 55 nm), in order to reduce the parasitic inductance.

The maximum thickness of crack-free films grown on bare silicon substrates is ~ 70 nm, due to thermally induced film stress. Task 3 of this program was to investigate various methods that could help relieve the film stress, however, we felt a suitable fallback would be to fabricate junctions on SOS wafers, which could support thicker YBCO films than Si. (The thermal expansion coefficient of sapphire is much closer to YBCO than that of Si. The effect of the thin Si layer on the SOS is considered negligible.) SOS is also desirable due to sapphire's low dielectric constant (~ 9), good mechanical strength and the potential for superconducting and semiconducting device integration.

Figure 3 presents the resistance vs temperature for a ~ 160 nm thick YBCO film grown on YSZ-buffered SOS. As with the films grown on Si, the zero resistance T_c is measured to be 87.5 K with a width (10 – 90%, ΔT_c) of < 1 K. Scanning electron microscopy (SEM) showed no evidence of film cracking.

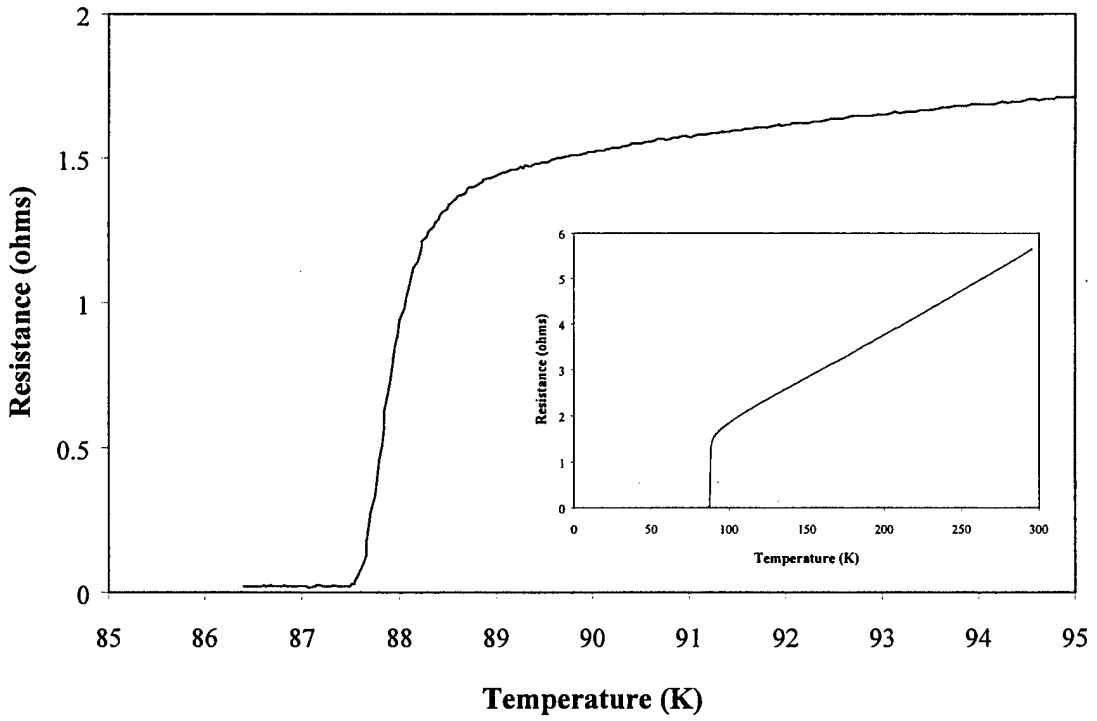

Figure 3. Resistance vs temperature for a 160 nm YBCO film grown on YSZ-buffered silicon-on-sapphire (SOS).

YBCO Films Grown at Conductus – Another goal of this task was to transfer AFR's technology for growing YBCO on Si to Conductus, thus allowing us to evaluate junctions produced on films grown by co-evaporation. The Conductus system uses sequential deposition and oxidation, involving reactive co-evaporation from elemental sources and a rotating oxygen-pocket heater. The first step was for Conductus to demonstrate growth of YBCO on buffered Si using their co-evaporation technique. At the

time, Conductus was not equipped to deposit the necessary YSZ buffer layer, therefore AFR supplied Conductus with some YSZ-coated Si samples. For YBCO growth, Y and Cu were evaporated using electron-beam sources and Ba from a thermal evaporation source. The substrate temperature was estimated to be 700 °C with a partial pressure of O_2 of 8 mTorr in the heater. For comparison, Conductus also deposited YBCO on single crystal YSZ substrates, as discussed below.

Conductus was not able to deposit good quality YBCO directly on the AFR YSZ-coated Si. The resistivity was more than ten times higher than that of films typically grown on the YSZ substrates and a relatively low T_c of 78 K was obtained. Figure 4 presents a XRD two-theta scan for the YBCO/YSZ/Si sample. There appears to be significant reaction at the YSZ/YBCO interface as evidenced by a $BaZrO_3$ peak in the x-ray. Following this result, it was decided to grow 200 Å of CeO_2 as an additional buffer on top of the YSZ/Si substrates in order to reduce the interface reaction. The structure and transport properties were much improved with the addition of the CeO_2 layer. Conductus then prepared a series of films of different thicknesses using the additional CeO_2 layer. For comparison, they also deposited simultaneously during each run a film on YSZ single-crystal substrates. Table 1 summarizes the properties of the YBCO films prepared at Conductus.

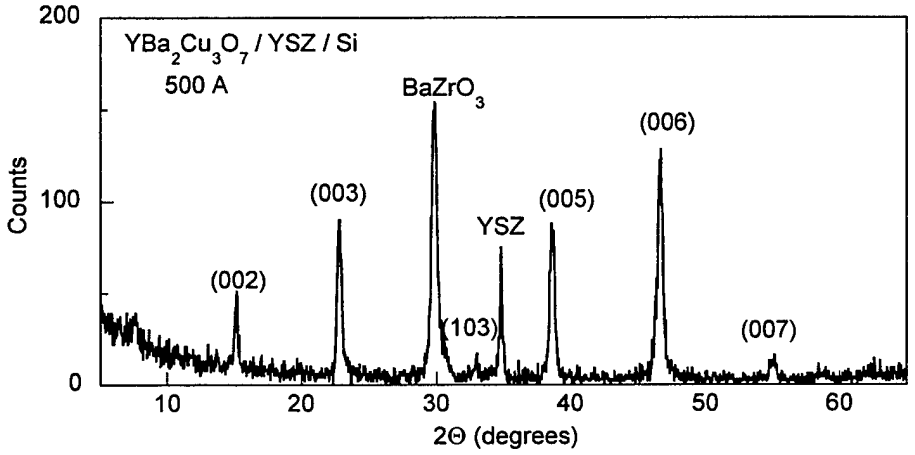

Figure 4. Two-theta scan for YBCO film grown at Conductus on AFR's YSZ-coated Si(100).

Table 1. **Summary of film properties of YBCO samples prepared at Conductus.**

Type	ρ (μΩ cm)	T_c (K)	Cracks	Comments
YBCO 500 Å /YSZ/Si	5000	78		large $BaZrO_3$ reaction
YBCO 500 Å /CeO_2 200 Å /YSZ/Si	340	88	no	small $BaZrO_3$ reaction
YBCO 750 Å /CeO_2 400 Å /YSZ/Si	500	82	yes	very small $BaZrO_3$ reaction
YBCO 1000 Å /CeO_2 200 Å /YSZ/Si	2100	80.5		small $BaZrO_3$ reaction
YBCO 500 Å /YSZ	285			no $BaZrO_3$
YBCO 750 Å /YSZ	260	87.2		no $BaZrO_3$
YBCO 1000 Å /YSZ	385	88		no $BaZrO_3$

The worst sample, was of course, the YBCO film grown directly on the YSZ-coated Si, having the highest resistivity ρ, the lowest T_c, and showing evidence of a large $BaZrO_3$ reaction. The YBCO film properties are improved with the additional CeO_2 buffer layer, which significantly reduces the $BaZrO_3$ reaction. Note that the transport properties of the 500 Å film, grown on CeO_2/YSZ/Si are comparable to those measured for the films grown on single crystal YSZ. Not surprisingly, the transport properties of the thicker films degrade significantly, which is attributed to stress-related microcracks.

It is not completely clear why Conductus was not able to grow good quality YBCO directly on our YSZ-coated Si, however, we suspect that the reason was related to their lack of capability to deposit YSZ films. Fork et al. [8] showed that removing YSZ films from the growth chamber and then reinserting in the chamber for YBCO growth seriously degrades the structure of the YBCO film. However, if an additional thin layer of YSZ is grown prior to the YBCO growth, the film structure is restored.

E-Beam Junction Fabrication Studies – In general, high-T_c Josephson junctions can be fabricated from grain boundaries, nanobridges, proximity effect, tunneling, or weakened structures. One of the simplest methods of HTS JJ fabrication is that in which a weak link is created by focused electron irradiation [9,10]. The e-beam method has been proven to possess a great deal of flexibility in positioning the junctions on chips and in controlling the junction parameters. As a result, it has been found to be successful in fabricating various circuits with HTS JJ's [11,12]. Junction performance depends in large part on the properties and size of the irradiated region in the direction of transport current. Upon irradiation, oxygen atoms in YBCO are displaced into interstitial positions. Chain oxygen disordering or plane oxygen defect formation can take place, depending on oxygen contents and e-beam incident energies. As a consequence, within a YBCO film, there are regions that are either slightly or heavily damaged. Although e-beam-made junctions have been shown to behave close to the resistively shunted junction (RSJ) model and to possess the uniform critical current density, there is a lack of understanding of the nature of the junctions and their physical properties. In order to refine the junction fabrication process, part of SUNY's efforts were focused on these issues.

The samples studied here were c-axis oriented YBCO (25 nm thick) grown on $LaAlO_3$ substrates by the BaF_2 process. Films were fabricated into microbridges by conventional photolithography using PMMA resist and wet etch (0.02% HNO_3 in DI water). The typical microbridge length was ~4 μm and width ~ 3 μm. Each microbridge was further modified by a process referred to as direct electron beam writing, using a Philips CM-12 electron microscope with a LaB_6 cathode. After writing, the temperature dependencies of the resistance and voltage vs. current V(I) characteristics of the modified microbridges (e-beam junctions) were measured. In a few experiments, YBCO films patterned into a six-probe configuration were uniformly irradiated. A complete set of resistivity, Hall, V(I) measurements was performed on these films and followed by annealing at different temperatures in He atmosphere. These measurements were intended to obtain more information on stability and annealing kinetics of the e-beam damaged YBCO.

In order to better understand and be able to control the properties of e-beam junctions a quantitative description of the e-beam writing process, including a description of the electron beam, was developed at SUNY. According to the microscope manufacturer, the electron density in the beam has a gaussian distribution with the full width at half maximum value (FWHM) specified as the geometric (nominal) spot size, b_g. Hence, the beam current density in the focal plane is given by $j_g = j_0 exp(-r^2/b^2)$, where $b = b_g/2(\ell n2)^{1/2}$ and r is the distance from the beam center. At the geometric spot size used (b_g=1.5 nm), b is 0.9 nm. This narrow gaussian distribution can be attributed to the bright central part of the beam as was observed in TEM mode. There was also a less intense but much broader component of the beam (halo), most likely caused by spherical aberration in the probe-forming lens. The current distribution in this halo can be described by another gaussian $j_{sh} - j_1 exp(-r^2/b_1^2)$ with the FWHM given by $0.5C_s(d_2/f)^3$, where C_s is the coefficient of spherical aberration of the objective lens, d_2 is the diameter of the condenser aperture,

and f is the focal length of the objective lens. At d_2=100 μm, parameter b_1 in the microscope used is 30 nm. This agrees reasonably with the size of the halo observed in the TEM mode.

The concentration of in-plane oxygen defects induced in the YBCO is shown in Figure 5 as a function of the distance from the e-beam-written line. The distribution of defects resembles the beam profile. There is a broad region of a relatively low concentration of defects produced by the halo, which is superimposed with the narrow region of high defect concentration produced by the narrow component of the beam. The size of each region is set by, respectively, the narrow and broad compoents of the incident beam. Since the induced defects are pair breakers, it is clear that the superconducting order parameter should be somewhat suppressed at distances ~ b_1 and be strongly suppressed in the region of the high concentration of defects. One could, in principle, solve microscopic equations of superconductivity with this distribution of pair breaking defects, find the y-dependence of the order parameter $\Delta(y)$, and calculate the critical supercurrent of the junction. This is, however, a formidable undertaking. A simplified model is described below.

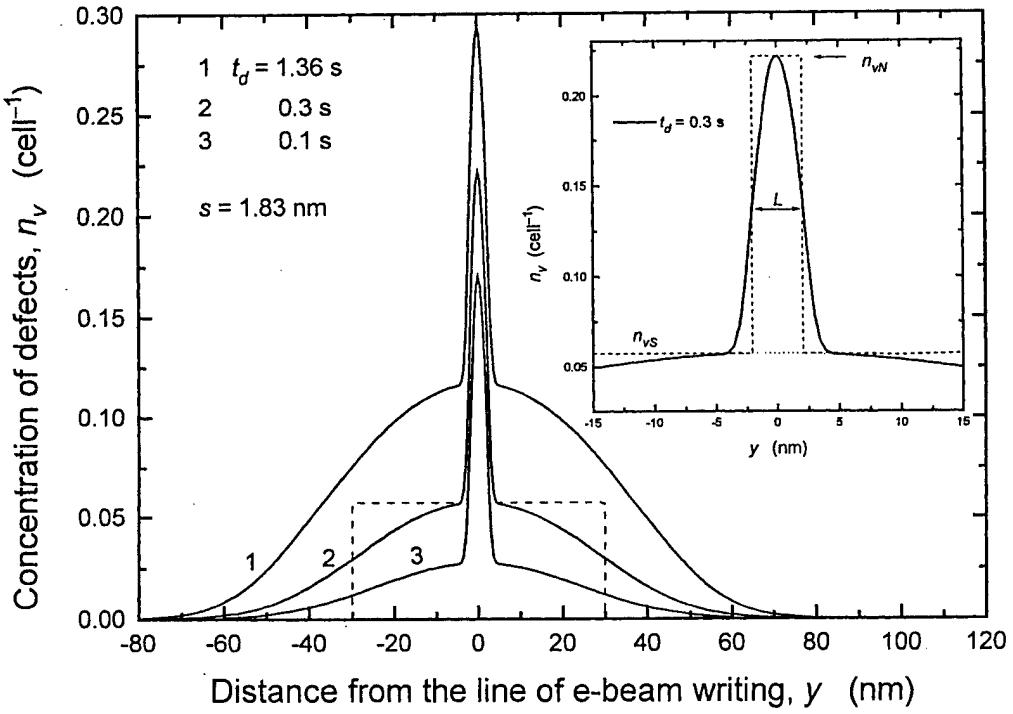

Figure 5. Calculated distribution of the induced defect concentration in the e-beam junction. Different curves correspond to different writing times at the same beam current, spot size, and magnification.

In the region of light damage, the concentration of defects changes on a much larger scale than both the coherence length ξ_0 and the mean free path. We may therefore regard this region as a nonuniform superconductor in which the local critical temperature $T_c(y)$ is determined by the local concentration of pair breaking defects. The local critical temperature is given by a solution of the equation:

$$\ln\frac{T_c}{T_{c0}} = \psi\left(\frac{1}{2}\right) - \psi\left(\frac{1}{2} + \frac{2\delta T_c n_d}{\pi^2 T_c}\right) \quad (1)$$

Where ψ is the digamma function, T_{c0} is the criticla temperature in the pure superconductor, n_d is the concentration of pair breaking defects, and δT_c is the parameter characterizing the rate of T_c reduction at low concentration of defects, $T_c = T_{c0} - \delta T_c n_d$. The induced defects are in-plane oxygen vacancies, $n_d \equiv n_v$, in which case $\delta T_c = 280$ K per defect in the unit cell [12]. The $T_c(y)$ dependences computed form Eq. (1) are shown in Figure 6. One can see a significant reduction of T_c of the film near the barrier (region of heavy damage) which is completely determined by the broad component of electron beam. Also shown is the $T_c(y)$ dependence in the region of heavy damage, which indicates what would be the critical temperatures of the bulk superconductor with such a concentration of in-plane oxygen defects.

As shown in the inset in Figure 5, the concentration of induced defects is almost constant near the barrier on a scale of several hundred angstroms. Accordingly, the critical temperature (denoted as T_{c1} in Figure 7, below) is also nearly constant on the same scale. Thus, a simplified model can be constructed by substituting the actual distribution of defects on two step-wise functions, as shown in Figures 5 and 6. This leads to an $SS_1"N"S_1S$ structure, where S refers to the undamaged film (critical temperature T_{c0}) far from the junction, S_1 refers to the region of weak, nearly uniform damage in the vicinity of the barrier (critical temperature T_{c1}), and *"N"* is the barrier (critical temperature T_{cN}).

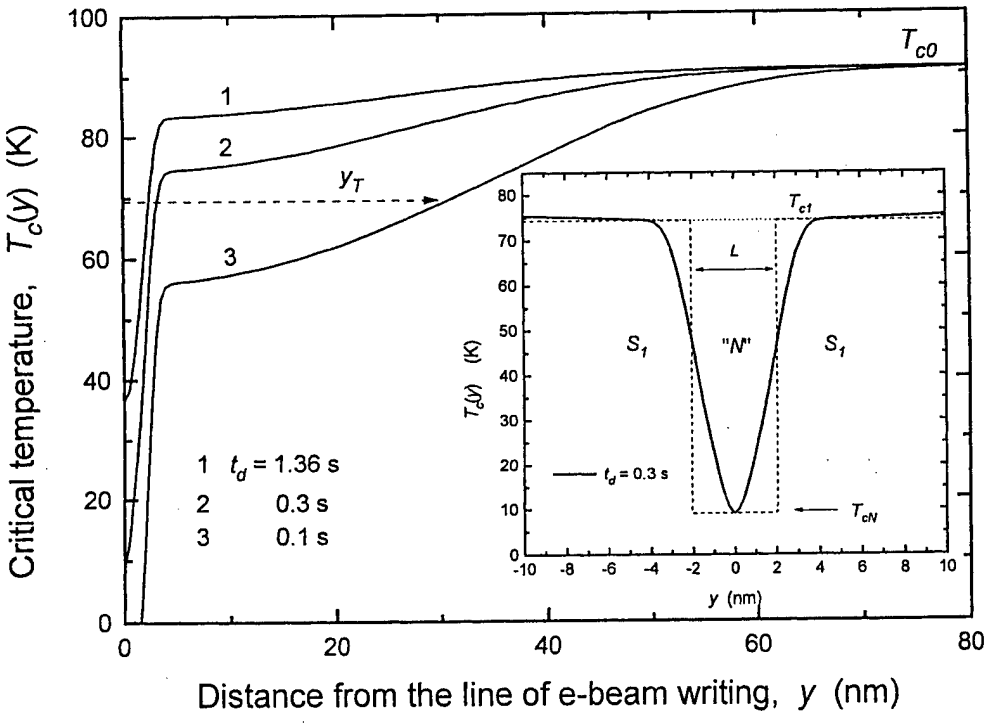

Figure 6. Calculated critical temperature of the YBCO film in the region of and near the e-beam written junction. Curves 1 to 3 correspond to the same e-beam writing parameters as in Fig. 5.

Two important parameters are the critical temperature T_{c1} and the thickness of the barrier. The effective thickness of the barrier (length of the junctions) L can be defined as the FWHM, i.e., $L/2$ is the distance at which the concentration of defects is half of $n_v(0)$, roughly, $L \approx b^*[2v_r n_v(0)]^{1/2}$. Thus defined L was calculated to be about 5 nm for all the studied junctions. This value agrees with other estimates of the junctions length coming, e.g., from the I_cR_N product and its temperature dependence.

Figure 7 shows the critical temperatures (defined as onset temperature of the critical current T_{on}) for the set of e-beam junctions along with the calculated critical temperature T_{c1} (as defined in Figure 7). The experimental and calculated values agree remarkably. This strongly suggests that T_{on} is the actual superconducting critical temperature of YBCO in the vicinity of the barrier. Suppression of the junction critical temperature is obviously an unwanted effect. In the picture developed it is caused by the broad component of the electron beam and in principal could be diminished by better defining the beam profile, e.g., by component scales as the square of aperture diameter d_2^2. Therefore, one needs to increase proportionally the writing time in order to maintain the same density of defects in the barrier or to use a higher brightness cathode.

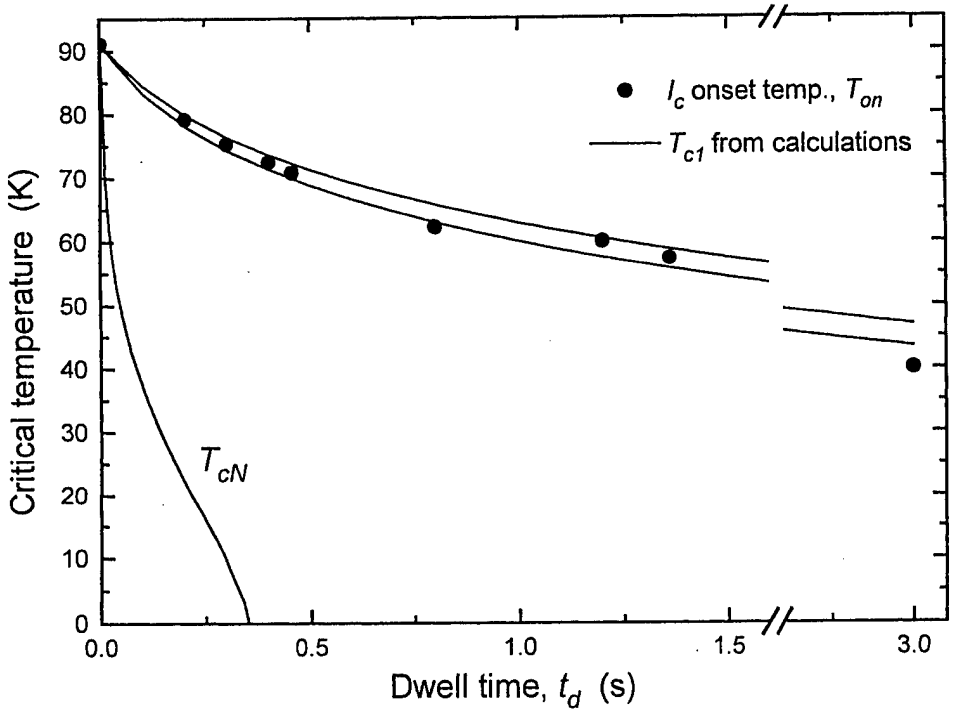

Figure 7. The onset temperature of the critical current in the e-beam junction (•) as a function of writing time (dwell time per stop-point). The results of model calculations for the superconducting critical temperatures of the junction banks, T_{c1}, and of the barrier, T_{cN}, correspond to the actual stop point separation s = 1.83 nm, the estimated effective beam width b^* = 1.5 nm, the estimated halo width b = 30 nm, and the actual beam current 0.55 nA. There is about 5% spread in the onset temperature of the junctions prepared under nominally identical conditions. The two computed T_{c1} curves show the lower and upper boundaries set by the uncertainty in determination of the e-beam parameters.

Further development of the e-beam writing process included studies of the critical current, I_c and the normal resistance, R_N. Regarding resistance, the typical temperature dependence is shown in Fig. 8. At a temperature T below the superconducting transition T_{c0} of the YBCO film, the measured resistance can be viewed as a series resistance of the barrier (i.e., the heavily damaged region) and those parts of the film in the vicinity of the barrier whose critical temperature is lower than T. As the temperature decreases further, more portions in the film become superconducting and the normal region gradually shrinks approaching the size of the heavily damaged region. In the local approximation, the total resistance can be expressed as:

$$R_N A = 2\int_0^{y_N} \rho(y)dy, \qquad (2)$$

where y_N is the position of the SN boundary at temperature T, i.e., a distance at which $T_c(y_N) = T$. The $\rho(y)$ is the local resistivity determined by the local concentration of defects, and A is the junction area. The resistivity of irradiated YBCO can be expressed as $\rho = \rho_0 + \alpha T$, where the residual resistivity is proportional to the concentration of in-plane defects, $\rho_0 = \delta\rho_d n_v$, and the temperature coefficient α is almost independent of in-plane defect concentration as shown in our previous work. It was found to be 1.5 mΩ•cm per in-plane oxygen defect in the unit cell, and the typical value for α is 1.4 μΩcm/K. Using these parameters and the calculated distributions of the concentration of induced defects $n_v(y)$ and the local critical temperature $T_c(y)$, we computed $R_N(T)$. The result is shown in Figure 8 by two solid lines reflecting the uncertainty in the parameters. The experimental data are shown by solid circles.

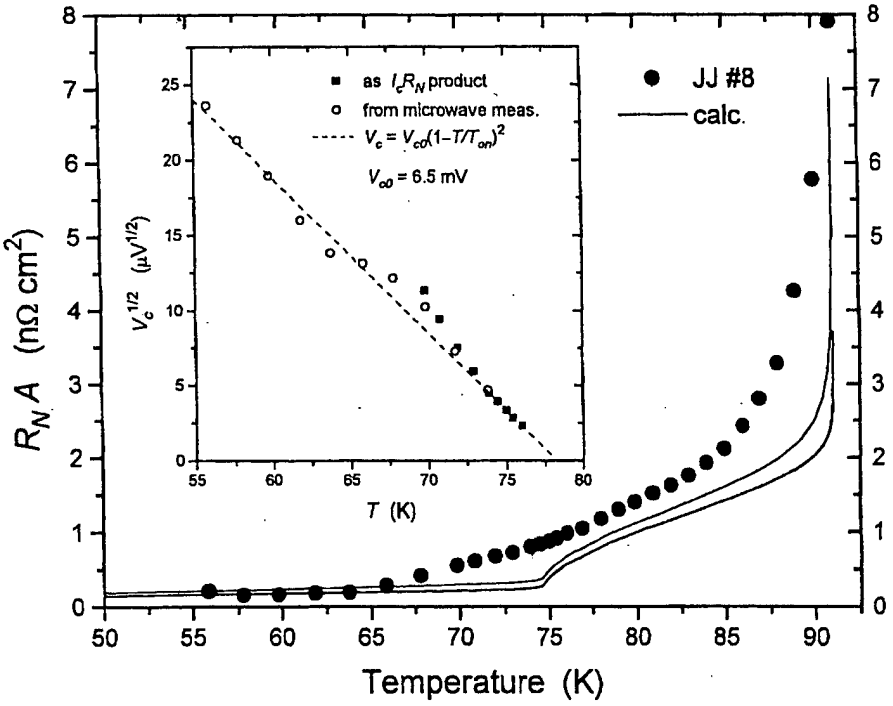

Figure 8. The temperature dependence of the normal resistance of Josephson junctions.

As can be seen, there is good agreement between calculated results and experimental data at temperatures somewhat below the onset of the critical current at T_{on}, yet the calculated resistance is systematically lower than the measured one at temperatures around and above the onset temperature. This is probably caused by the underestimation of any of the following: spread of the damage, local resistivity, and contribution of the heavily damaged region. For instance, a broader transition at T_{c0} in the experiments than the calculated values may indicate that e-beam damage spreads over a wider region, possibly due to the influence of back-scattered electrons. Moreover, the calculated $R_N(T)$ has a feature at around 75 K, which reflects the superconducting transition near the barrier. In contrast, the measured resistance smoothly crosses over this temperature range.

Another prime characteristic is the critical current density j_c and its temperature dependence. In the simplest case of the uniform current distribution, the critical current density is readily found as I_c/A. However, when the critical current is limited by the self-field effect (which is always the case in junctions with high critical currents), a more complex analysis is required. Without going into details, the result of this analysis is shown in Figure 9 by solid squares and for comparison, the apparent critical current density (I_c/A) is represented by open circles. The calculated critical current density is also plotted as a solid line, which was derived without any fitting parameters from the conventional proximity effect theory with soft boundary conditions. All the necessary parameters such as the junction length L, the critical temperature near the barrier T_c, the proximity effect parameter γ, and the coherence length ξ_N were also calculated. The good agreement between the experimental data and the calculation illustrated in Figure 9 again supports the correctness of our description and understanding of the e-beam junction properties.

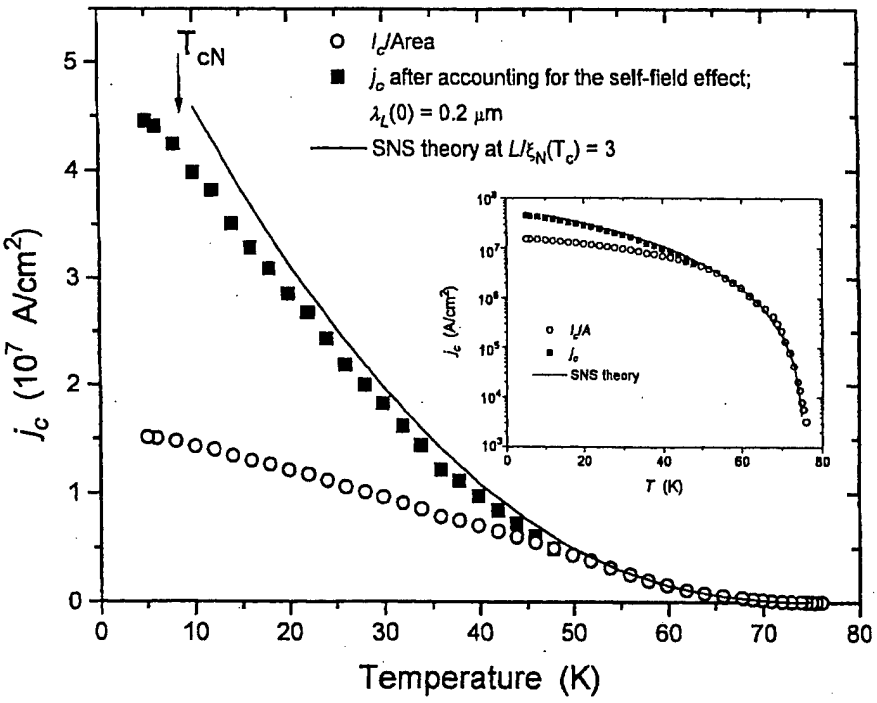

Figure 9. The temperature dependence of the critical current density of Josephson junctions.

This model hence can serve as a reliable basis for the description of e-beam junctions. It also accounts for the influence of various microscope parameters on the final properties of the junctions. In turn this allows for better control of the technological process and, as a result, better reproducibility and predictability of the devices.

Task 2: Junction Stability through Improved Chemistry - To improve the thermal stability of the e-beam modified junctions.

In Phase I, the Josephson junctions fabricated via electron beam irradiation were susceptible to slow drift in parameters at room temperature, which implied junction instability and thus would limit their applications. There are two possible sources of junction instability – diffusion of induced defects out of the irradiated region and recombination of defects inside the region. Both factors could be difficult to separate experimentally because the process of recombination also involves diffusion, i.e., a displaced oxygen needs to diffuse close to a vacancy in order to recombine. According to SUNY's study on YBCO films, the typical activation energy governing the junction annealing is about 1.1 eV. This value is close to the oxygen diffusion activation energy found in many experiments. Therefore, it is likely that the rate of diffusion controls annealing. As a consequence, one would like to increase the oxygen diffusion activation energy by modifying the lattice crystal potential near the planes or the chains. This can be achieved by several ways and one of which is by chemical substitution. For instance, Co can substitute for Cu in chain positions ($YBa_2Cu_2Cu_{1-x}Co_xO_7$), which decreases dramatically the diffusion of chain oxygen. However, Co substitution also reduces carrier concentrations and thus T_c values. On the other hand, one can substitute Y and/or Ba with Ca and/or La, respectively, to vary the crystal potential near the plane. $Y_{0.6}Ca_{0.4}Ba_{1.6}La_{0.4}Cu_3O_7$ has been found to be much more stable with respect to environmental degradation [13]. The goal of this task was to investigate different approaches of improving the junction stability including (1) optimization of e-beam irradiation conditions, (2) doping YBCO with certain elements, (3) implementation of alternative YBCO film treatment processes, and (4) fabrication of Josephson junctions from alternative HTS films, for example, $Bi_2Sr_2CaCu_2O_8$ (BSCCO) and (Bi, $Pb)_2Sr_2CaCu_2O_8$.

As part of this task, SUNY studied the annealing kinetics (stability) of the e-beam-irradiated YBCO films on $LaAlO_3$ to serve as background measurements needed for the comparison with data on the stability of substituted YBCO films and films on Si substrates. In order to have a well-defined geometry and achieve higher sensitivity, the measurements were performed on films patterned into a 10-μm wide strip (current channel) with four potential probes 10 μm apart. The area of the strip was uniformly irradiated by 120 keV electrons in a Philips CM-12 electron microscope. Figures 10 and 11 show, respectively, the time variation of the resistance per square and the critical temperature of an irradiated 50-nm thick YBCO film annealed at 325 K in He atmosphere. The annealing was interrupted by several cooling-warming cycles during which the critical temperature was measured. The time evolution of the critical temperature can be well described by the so-called stretched exponential kinetics

$$T_c(t) = T_c(inf) - [T_c(0) - T_c(inf)]\exp(-t/\tau)^{\beta}, \qquad (3)$$

Where $T_c(0)$ is the critical temperature right after the irradiation, $T_c(inf)$ is the critical temperature after an infinitely long annealing, τ is the relaxation time, and β is a parameter. If a complete annealing of defects can be achieved, $T_c(inf)$ should presumably coincide with the critical temperature of the non-irradiated material. The best fit to our data gives $\tau = 767$ min, $\beta = 0.424$, and $T_c(inf) = 89.9$ K that is close to the T_c in a non-irradiated film, 90.2 K. The time variation of the resistance is far more complicated. Several factors could contribute to that. First, we found that the cooling-warming cycle increases the resistance of the film perhaps due to accumulation of some stresses in the film. Annealing of these stresses is characterized by its own kinetics that seems to be a simple exponential. This process superimposes the main annealing kinetics of irradiation defects and thus complicates the analysis. Second, for a long annealing time, some resistance oscillations were observed, which might indicate the existence of a more complex process than a simple recombination of vacancy-interstitial pairs. Third, we found some difference between anneals with the transport electric current on and off. This could be due to electron diffusion. However, all these issues require a more detailed investigation.

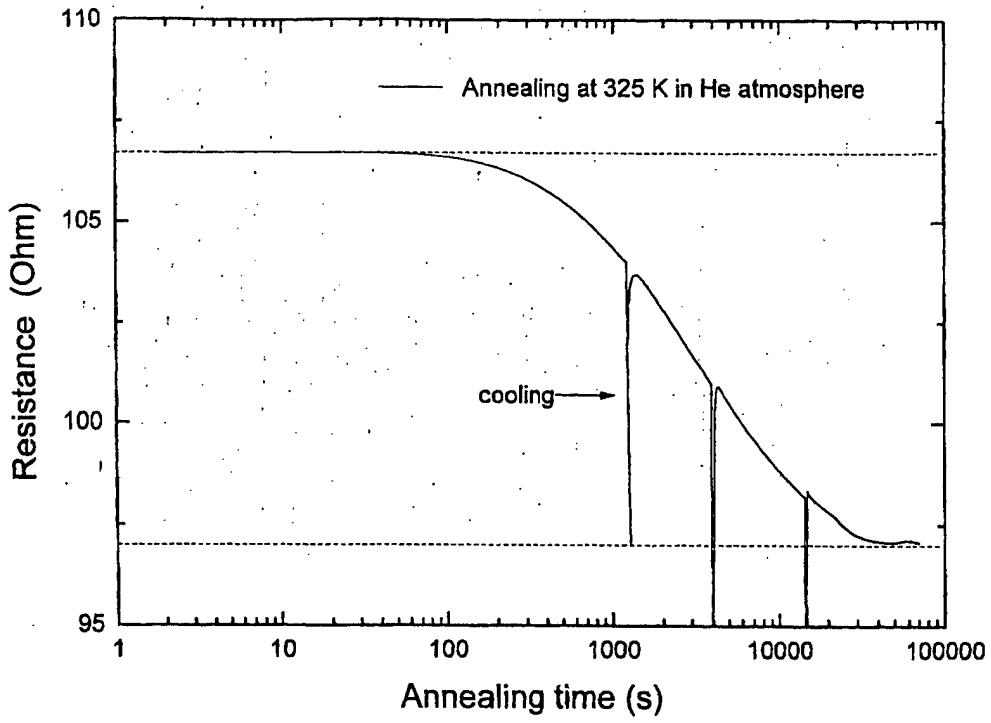

Figure 10. The time variation of the resistance per square of an irradiated 50-nm-thick YBCO film annealed at 325 K in a He atmosphere.

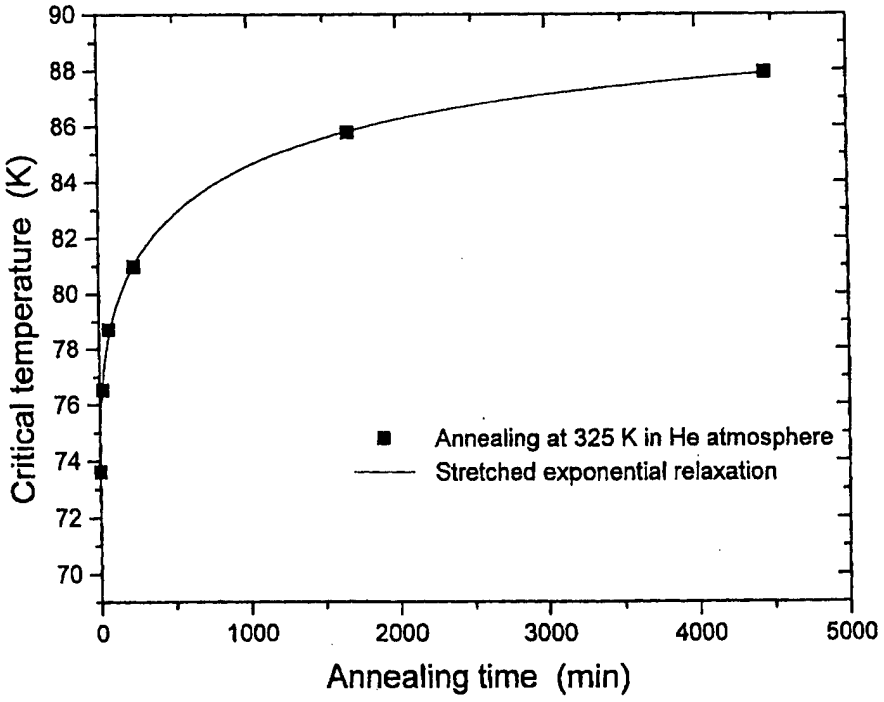

Figure 11. The time variation of the critical temperature of an irradiated 50-nm-thick YBCO film annealed at 325 K in a He atmosphere.

AFR did some work depositing films of $Y_{1-x}Ca_xBa_2Cu_3O_{7-\delta}$ (YCBCO, x = 0.1) and BSCCO onto Si substrates. Most of the work concentrated on depositing these HTS materials using the YSZ buffer layer employed for growth of the standard YBCO on Si. Although, we were able to grow superconducting YCBCO films (using deposition conditions for unsubstituted YBCO), the critical temperature of our best film was unacceptably low, ~77.5 K, with a fairly broad transition of ~ 6 K, as shown in Figure 12. For BSCCO, we were even less successful, and were not able to demonstrate growth of superconducting films (> 77 K) on YSZ-buffered Si.

The limited work that was done on these HTS materials was by no means optimized. Regarding the YCBCO, we believe that adjustment of deposition parameters (substrate temperature, laser fluence, deposition rate, etc.) would be necessary, and also the use of the added CeO_2 layer would be worth exploring. For the BSCCO, we felt that alternative buffer layers, such as MgO and $SrTiO_3$ would enable improved growth. In fact, we began investigating growth of MgO on bare Si by PLD. Following the method of Fork et al. [14], which utilizes a pure Mg target, we were able to demonstrate epitaxial growth of MgO thin films on Si. Figure 13 displays XRD patterns obtained for a MgO film grown at ~ 425 °C at the deposition system base pressure of 5 x 10^{-6} Torr. In the two-theta scan (Figure 13a), only the MgO (002) peak is observed and the peaks only at 90° intervals in the phi scan (Figure 13b) confirm epitaxy.

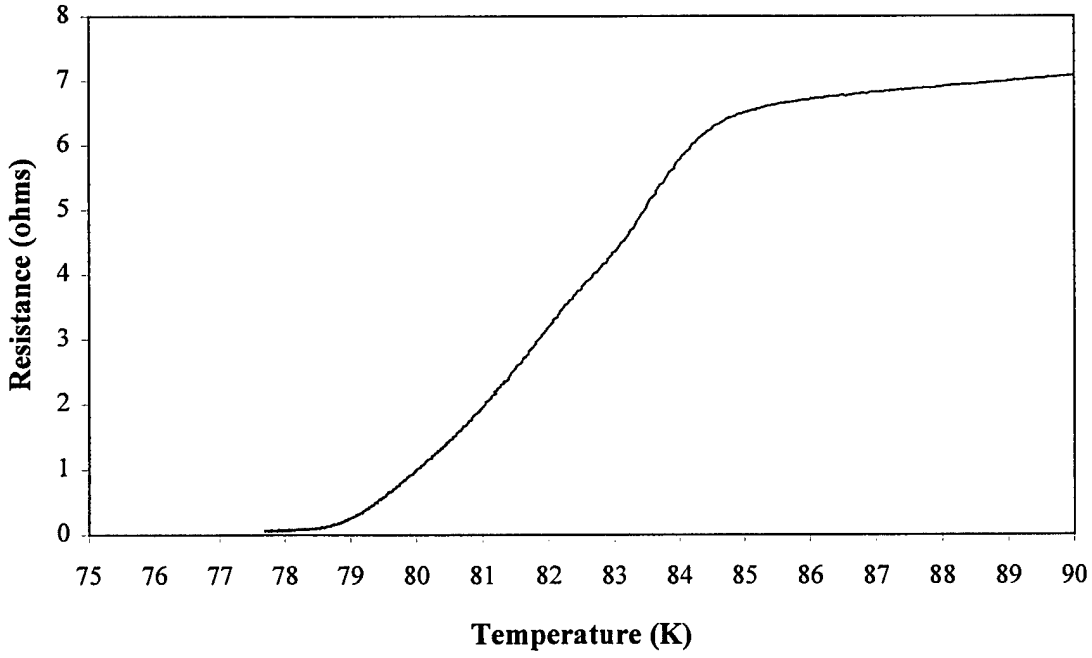

Figure 12. Resistance vs temperature for a 50 nm YCBCO film grown on YSZ-buffered silicon. (The resistance is not zero due to a baseline offset in the measurement.)

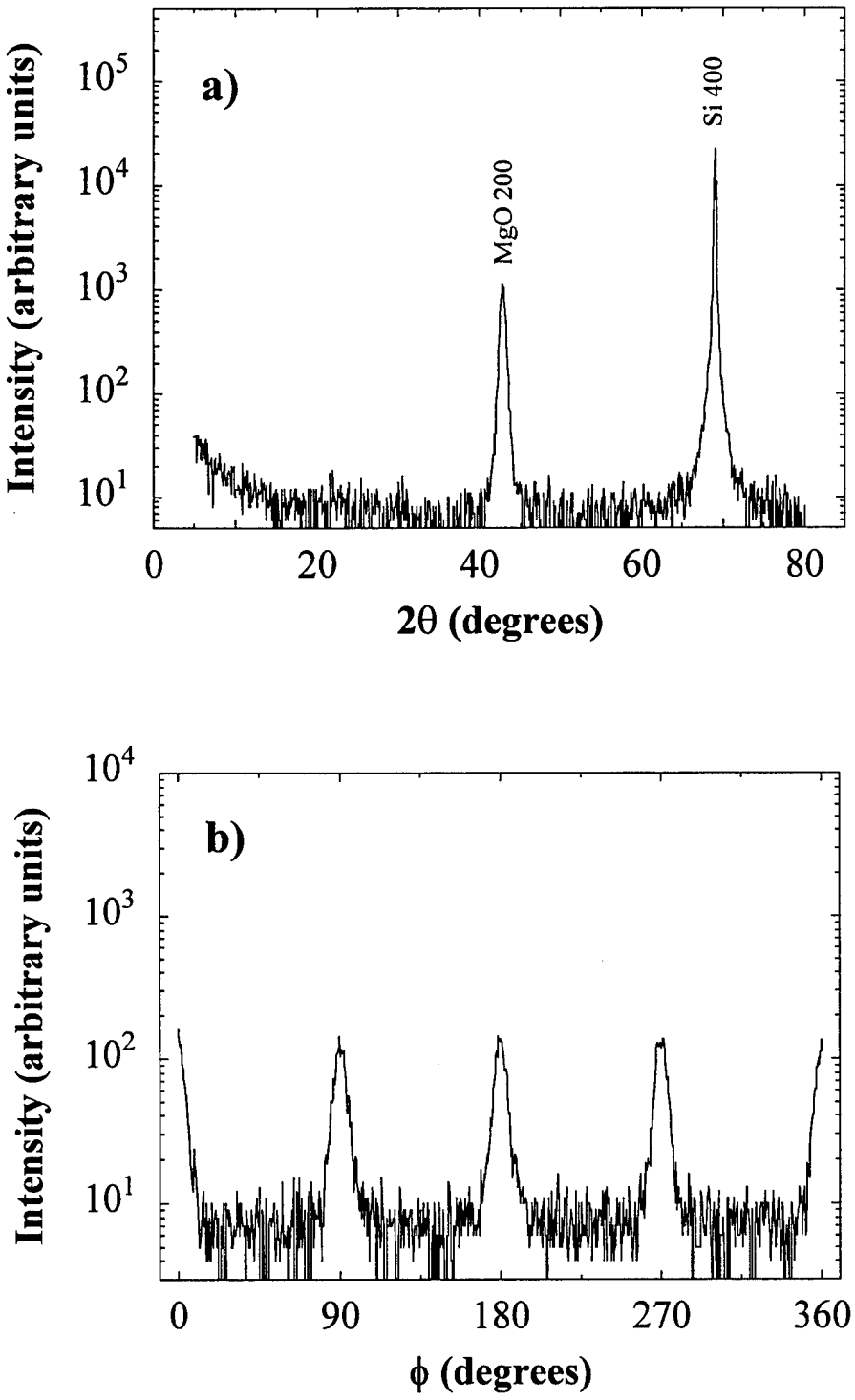

Figure 13. XRD patterns for a MgO film grown on Si in base pressure of 0.5 x 10^{-6} torr at a substrate temperature of ~ 425 °C, a) two theta scan, b) phi scan of the MgO {202} family of reflections.

Table 2 lists XRD data from several MgO/Si films studied in this task. The films were grown in pressures ranging from 5 x 10^{-6} (base pressure) to 5 x 10^{-3} Torr at three different temperatures. To evaluate the film quality, ω-rocking curve full widths at half maximum (FWHM) were measured on the MgO (002) reflection to characterize the out of plane misalignment of the MgO grains. As can be seen from Table 2, the best MgO film was grown at ~ 450 °C in 5 x 10^{-3} Torr O_2 and the sensitivity of the film quality to O_2 pressure and substrate temperature is quite evident, which is consistent with Fork et al. Even so, the FWHM of the rocking curve is still fairly broad at 2° (the FWHM of our YSZ films on Si is routinely 1° or better), indicating the need for continued optimization of the deposition parameters. Unfortunately, as is explained in detail in Task 5, continued work in this task was halted because of equipment and personnel problems that occurred at SUNY during this program.

Table 2. **XRD Measurements for MgO films grown under different deposition conditions.**

Substrate Temperature (°C)	O2 Pressure (mTorr)	Rocking Curve Width (Δω)
725	0.5	. . .
450	0.5	2°
450	0.05	2.2°
450	0.005	2.9°
350	0.05	3.7°
350	0.005	4.8°

Task 3: Device Integration - to develop the capability of integrating the junctions onto rf-compatible substrates with wiring, ground-plane and crossover structures.

Film stress is a major issue for HTS devices on silicon substrates. Silicon has a smaller thermal expansion coefficient ($3.8 \times 10^{-6}\ °C^{-1}$) than that of YBCO ($16 \times 10^{-6}\ °C^{-1}$) [15] which in general, puts the YBCO film under severe tensile strain during cool-down from the growth temperature. At thicknesses beyond 70 nm, YBCO films grown on YSZ-buffered silicon relieve stress by cracking, which results in degradation of superconducting properties and premature aging [15]. This present thickness limitation on silicon has several application-killing consequences. Multi-layered wiring, crossovers and groundplanes are virtually impossible for films of this thickness. Also, because the superconducting London penetration depth is greater than the maximum crack-free film thickness, the parasitic inductance and surface resistance of HTS structures on silicon are increased. This will greatly complicate the design of RSFQ elements as well as degrade the performance of filters, resonators transmission lines and other passive components. For these reasons, the major goal of this task was to develop a compliant substrate methodology that would support high quality, low stress, crack-free YBCO on Si and other rf-compatible substrates, such as quartz. Given the availability of funds for this project, this was a high risk task. however, as stated earlier, we felt that the ability to deposit thicker YBCO on SOS was an acceptable fallback.

The basic idea behind using compliant substrates for heteroepitaxy of mismatched film/substrate structures, such as YBCO on Si, is to provide a flexible layer between the substrate and the device (YBCO) layer. Ideally, the flexible layer can expand or contract to accommodate lattice and/or thermal mismatch and can also support high quality epitaxial growth of the desired device layer. We investigated three methods of producing low-stress YBCO films of thickness > 70 nm onto silicon, 1) viscoelastic glass buffer layer, 2) CaF_2 buffer layer, and 3) film transfer. The first two methods fit the definition of a compliant substrate technology and involve the use of a thin buffer layer tailored to relieve stress accumulated during cool-down from the growth temperature. The third method, involving film transfer from one substrate to another, is an epitaxial lift-off technique performed after deposition. During the course of this program, we focused on the CaF_2 buffer method, which we felt was the most straightforward technique, and had shown promise in reducing stress in other mismatched materials by other researchers. Below, the viscoelastic glass buffer layer and film transfer methods are briefly described, followed by a detailed description of the work performed on the CaF_2 buffer method.

Viscoelastic Glass Buffer Layer – The basic idea with this method was to fabricate silicon on insulator (SOI) substrates (Si/glass/Si substrate), incorporating soft glass materials as the insulating layers. Here, the thin Si layer acts as a template for epitaxial growth of the YBCO/YSZ filmstack. During cooldown from the growth temperature, the viscoelastic glass layer deforms (at temperatures above its annealing point), acting to relieve the accumulating thermal shear stress between the YBCO and Si substrate. Below the annealing temperature, the glass buffer will exhibit elastic behavior, and stress will accumulate in the overlying film. Ideally, glass compositions, such as BPSG, would be chosen that yield the lowest annealing temperatures consistent with the requirements of the high growth temperature of the YBCO (~ 780°C). The anticipated fabrication sequence, which follows a standard bond and etchback process, can be summarized as follows:

1. Bond BPSG-coated Si to standard SOI (which incorporates a buried SiO_2 layer) in a high temperature furnace.
2. Remove bulk Si from standard SOI component of the bonded structure using a hot KOH solution.
3. Remove thin SiO_2 using a buffered HF solution.

Essentially, this transfers the thin, monocrystalline layer of Si from the commercial SOI wafer to the BPSG-coated wafer. In the limited attempts we made at fabricating this structure, we found step # 2 to be most difficult – typically the KOH etch was difficult to control using our crude etchback facilities, resulting in non-uniform etching. We eventually abandoned this idea in favor of the CaF_2 buffer method, which we felt would be easier to implement. Nonetheless, we still feel that this idea has merit and is worth further investigation.

Film Transfer - This method is an attractive epitaxial lift-off technique because it has the potential to mate HTS films such as YBCO with a variety of substrates including silicon, glass, and polyimide. The procedure was being developed by Dr. Chang-Beom Eom of Duke University and is as follows. An epitaxial $SrRuO_3$ etch-stop layer followed by the YBCO film are grown on a single-crystal (001) $SrTiO_3$ substrate. $SrRuO_3$ has been found to show excellent chemical stability and prepared as lift-off films [16]. The YBCO is then patterned, coated with an adhesive bonding agent, and bonded to a support wafer (sapphire has been employed for these experiments so far). The final step is to immerse the entire structure in an HF-based solution to chemically etch the $SrTiO_3$ substrate.

Through a small subcontract to Dr. Eom, we investigated the feasibility of this method. The focus was on selecting suitable adhesives that could survive the etchant solution. Different bonding agents were tried with varying degrees of success including crystal wax, crazy glue, GE varnish, all-purpose epoxy (Bowman No. 22013), and spin-on polyimide. The most successful bonding agent investigated was a HD Microsystems non-photosensitive polyimide (PI 2570) with an adhesion promoter (VM 652). The bonding strength was found to be good and did not degrade in the etchant. Unfortunately, the $SrRuO_3$ was not of suffcient quality and failed to act as an etch stop. We do believe, however, that using a high quality $SrRuO_3$ etch stop combined with the polyimide bonding agent should result in successful transfer of YBCO films to other substrates. While our opinion was that this method warranted continued investigation, we felt that further work on this method was beyond the scope of the program.

Calcium Fluoride Buffer Layer – For this program, we focused our efforts on developing a compliant substrate technology based on the use of a thin epitaxial CaF_2 buffer layer for the following reasons. The fluorides evaporate as undissociated molecules, thus films can be deposited stoichiometrically by some form of vacuum evaporation, such as thermal evaporation or molecular beam epitaxy (MBE) [17,18]. In addition, CaF_2 lattice matches well to Si (< 1 % mismatch), thus allowing high quality growth of epitaxial CaF_2 films on Si. From a processing point of view, we felt this would be an easier compliant substrate approach than the glass buffer layers. More importantly, CaF_2 has been observed to undergo plastic deformation, even at room temperature [19] and has, in fact, been suggested as a potential thermal expansion mismatch buffer for YBCO films grown on Si [20].

The thermal expansion coefficient of the Group IIa fluorides is significantly higher than Si, thus it would be expected that, assuming no mechanism for strain relief, CaF_2 thin films grown on Si would be under considerable tensile strain after cooldown from the elevated growth temperatures involved. However, strain relief has been observed for CaF_2 grown on Si [19]. Beyond a thickness of about 50 nm, the strain is shown to significantly decrease with increasing film thickness. CaF_2, in particular, exhibits no measurable strain for films 200 nm and thicker [21]. The strain relief is attributed to the movement of misfit dislocations near the fluoride/Si interface. CaF_2 has, in fact, been shown to undergo plastic deformation, i.e., release strain, even at room temperature [19]. CaF_2 has also been shown to relieve thermal strain in overgrown layers as well [19,22]. Schowalter et.al. [19] has compared strain measured for epitaxial GaAs films grown on Si(111) versus epitaxial GaAs grown on CaF_2/Si(111). Significantly higher levels of strain are observed in the GaAs layer when grown on bare silicon while the GaAs layers grown on the buffered silicon are strain-free.

Before attempting to deposit YBCO on CaF_2-coated Si, we felt that it was prudent to demonstrate epitaxial growth of YBCO with reasonable superconducting properties on single crystal CaF_2 substrates. 5 x 10 mm^2 chips of CaF_2(100) were purchased, several of which were sent to the Penn State for deposition of Y_2O_3 buffer layers in their MBE system. Since CaF_2 is reactive with YBCO under typical deposition conditions [23], a buffer layer is required. During the course of the Penn State work it was discovered that the CaF_2 crystal orientation was not (100) as specified but rather was (110). The supplier of the CaF_2 substrates acknowledged their mistake and agreed to replace all substrates purchased with chips of the correct orientation. The Penn State researchers later did successfully deposit epitaxial Y_2O_3 on the CaF_2(110) as determined by XRD. The samples were then sent to us for YBCO deposition as it was speculated that *c*-axis oriented YBCO may grow on CaF_2(110). Two samples of YBCO films were grown on those substrates and then characterized by x-ray diffraction. Neither film showed any evidence of YBCO growth; however, a weak BaF_2 peak was observed. Also, the Y_2O_3 layer appeared intact. The source of the fluorine is unclear since the buffer layer should prevent direct contact between the YBCO and the CaF_2. Possibly, the CaF_2 was oxidized to release fluorine as a gaseous product. Oxidation of the CaF_2 substrate may occur at the substrate edges, which are unprotected due to the non-conformal coverage of the MBE deposition flux.

After receiving more CaF_2 substrates with the correct (100) orientation, we decided to try growing YBCO using a YSZ buffer layer in our PLD system. The results obtained for YBCO films grown on YSZ-buffered CaF_2(100) at AFR were very encouraging as demonstrated by x-ray diffraction and T_c measurements. The YBCO film quality was studied as a function of deposition temperature and found, not surprisingly, to improve with increasing temperature. In each case, the YSZ buffer layer was grown under nominally the same conditions and was determined by XRD to be similar in quality for each sample.

The experimental procedure was as follows. The CaF_2 substrate is rinsed in acetone, isopropanol and reagent alcohol, spin-dried in nitrogen and bonded to a similarly cleaned Si chip with silver paint. The sample is then loaded into our deposition chamber, pumped down to base pressure and heated to ~ 300 °C for about one hour. The substrate is quickly heated to ~ 800 °C, at which point deposition of the YSZ buffer layer (~ 200 nm) begins. Oxygen is *immediately* introduced into the chamber at a pressure of .4 mTorr. Substrate temperature is determined by viewing the silicon chip with a pyrometer although we estimate that the actual temperature of the CaF_2 substrate may be up to ~ 25 °C lower than the Si. (All temperature values reported here, where YBCO was grown on YSZ-buffered CaF_2, are of the Si support chip.) Following the YSZ deposition, the chamber pressure is raised to 200 mTorr O_2 and the substrate temperature is adjusted to the desired temperature for YBCO deposition. Following the YBCO deposition, the chamber pressure is raised to 400 Torr O_2, the substrate temperature is quickly lowered to ~ 500 °C where it is held for 15 minutes and then cooled to room temperature. (Note that these deposition conditions are very similar to those we employ to grow YBCO on YSZ-buffered Si.)

Figure 14 presents x-ray diffraction results for a YBCO film (~ 150 nm thick) grown at 700 °C on YSZ-buffered CaF_2(100). From the two-theta scan (Fig.14a) it is shown that the YBCO is primarily c-axis oriented and that the YSZ is well oriented with respect to the substrate normal such that the following relationship exists:

$$(001)\text{YBCO} \,//\, (100)\text{YSZ} \,//\, (100)CaF_2$$

Figures 14b and 14c show phi scans of the YSZ (311) peak and the YBCO (103) peak, respectively, where phi = 0 along CaF_2 [311]. Peaks every 90 ° are shown for each layer, demonstrating in-plane epitaxy and that the YBCO is almost completely rotated 45° (i.e., single domain) in the plane with respect to the CaF_2 such that:

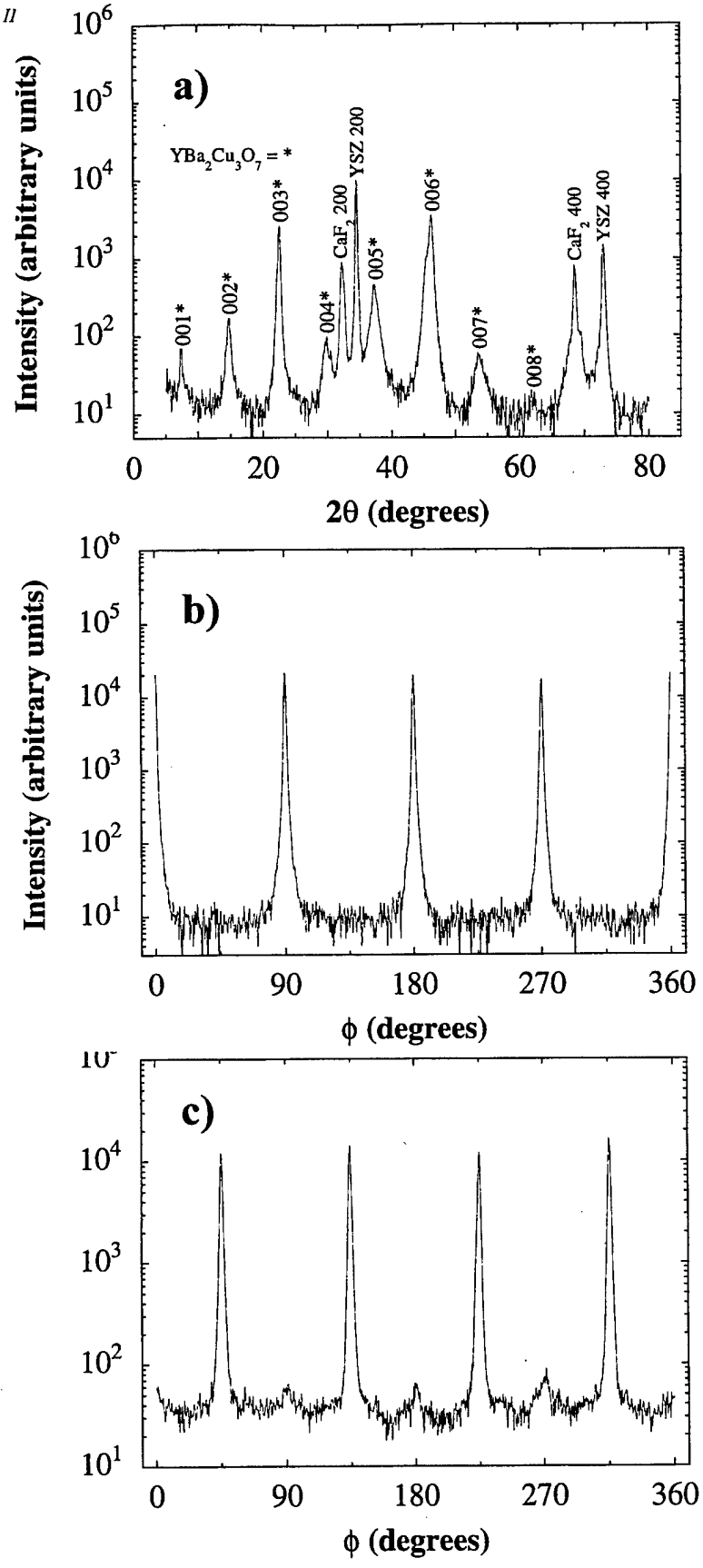

Figure 14. XRD patterns for a YBCO film grown at 700 °C on YSZ-buffered CaF_2(100): a) two-theta scan, b) phi scan of the YSZ(311) peak, and c) phi scan of the YBCO(103) peak.

[110]YBCO // [010]YSZ // [010]CaF_2

Rocking curves (not shown) were also measured for this sample. A FWHM of 0.63° obtained for the YSZ(200) peak indicates excellent crystalline quality, comparable to our best YSZ films grown on Si. A rather broad FWHM of 1.8°, however, is observed for the YBCO(005) peak, indicating relatively poor crystalline quality.

Figure 15 presents XRD patterns for a YBCO grown on YSZ-buffered CaF_2 at a deposition temperature of ~ 750 °C. Again, the film is primarily c-axis oriented and epitaxial, but, we note in the phi scan (Figure 15b) that a small component of twinning is present. The FWHM of the YBCO(005) peak (rocking curve, not shown) is 1.3°, is narrower than for the film grown at ~ 700 °C, suggesting improved crystalline quality. In addition, a four-point resistance measurement of another film grown at 750 °C demonstrated the film to be superconducting with a fairly low T_c = 81 K and a fairly broad transition width of about 4 K.

A Tc ~ 86.5 K was observed for a film grown at 785 °C and the crystalline quality of this film was superior to those grown at lower temperatures, as determined by XRD ω rocking curves (FWHM ~ 0.95°). Figure 16 presents XRD patterns obtained for this film. Although the out-of-plane alignment continues to improve with increasing temperature and the film is still epitaxial, we note substantial twinning (i.e., a mix of two domains) in the XRD phi scan (Figure 16b) which would be expected to have adverse effects on the device properties of this sample.

Raising the YBCO growth temperature to 810 °C continued this trend. The FWHM of the XRD ω rocking curve was ~ 0.82°, but as shown in Figure 17, we still observe a mixture of two domains - some of the YBCO is rotated 45° and some is cube on cube with respect to the YSZ/Si. These results were in contrast to the YBCO films we routinely deposit on YSZ-buffered Si at these growth temperatures, which are typically single domain and rotated 45° to the YSZ/Si. Clearly, the CaF_2 substrate was having a subtle effect on the YBCO deposition. Nonetheless, as shown in Figure 18, the resistance vs temperature is comparable to films grown on Si, with a Tc ~ 88.5 K along with a transition width of ~ 1 K.

To alleviate the twinning problem, two approaches were considered. First, on a YSZ-buffered CaF_2 substrate, we grew a YBCO film where we nucleated the first 20 nm of YBCO at 700 °C and deposit the remainder of the film (~ 130 nm) at 780 °C. XRD measurements, displayed in Figure 19, indicate improved YBCO crystalline quality (FWHM = 0.64 °) and that the YBCO is primarily single domain (note that there is evidence of some twinning, but it is a very small volume fraction exaggerated by the log scale of intensity) and rotated 45° with respect to the YSZ/Si. The two-theta scan does, however, reveal some minor impurities not observed in previous samples. Our second approach, which resulted in the best YBCO film so far in terms of structural quality, utilized a double buffer layer of YSZ followed by CeO_2 prior to YBCO deposition. The YBCO was then grown at 780 °C and again analyzed by XRD. Phi scans, presented in Figure 20, show the YBCO to be predominantly single domain and rotated 45° to the YSZ/Si. In addition, a rocking curve FWHM = 0.55° was obtained and no impurities were detected. No electrical measurements were performed in either case.

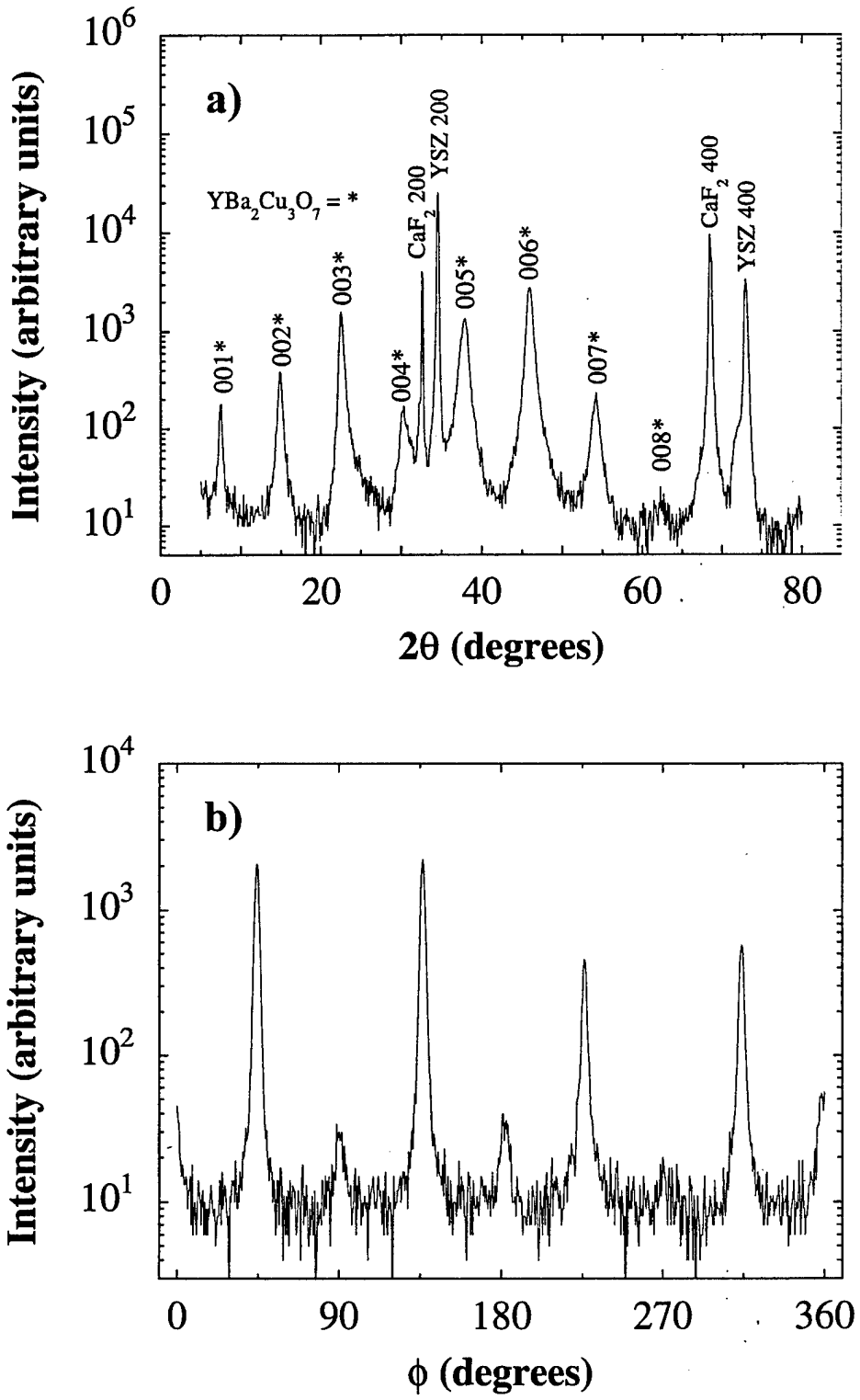

Figure 15. XRD patterns for a YBCO film grown at 750 °C on YSZ-buffered CaF_2(100): a) two-theta scan, b) phi scan of the YBCO(116) peak.

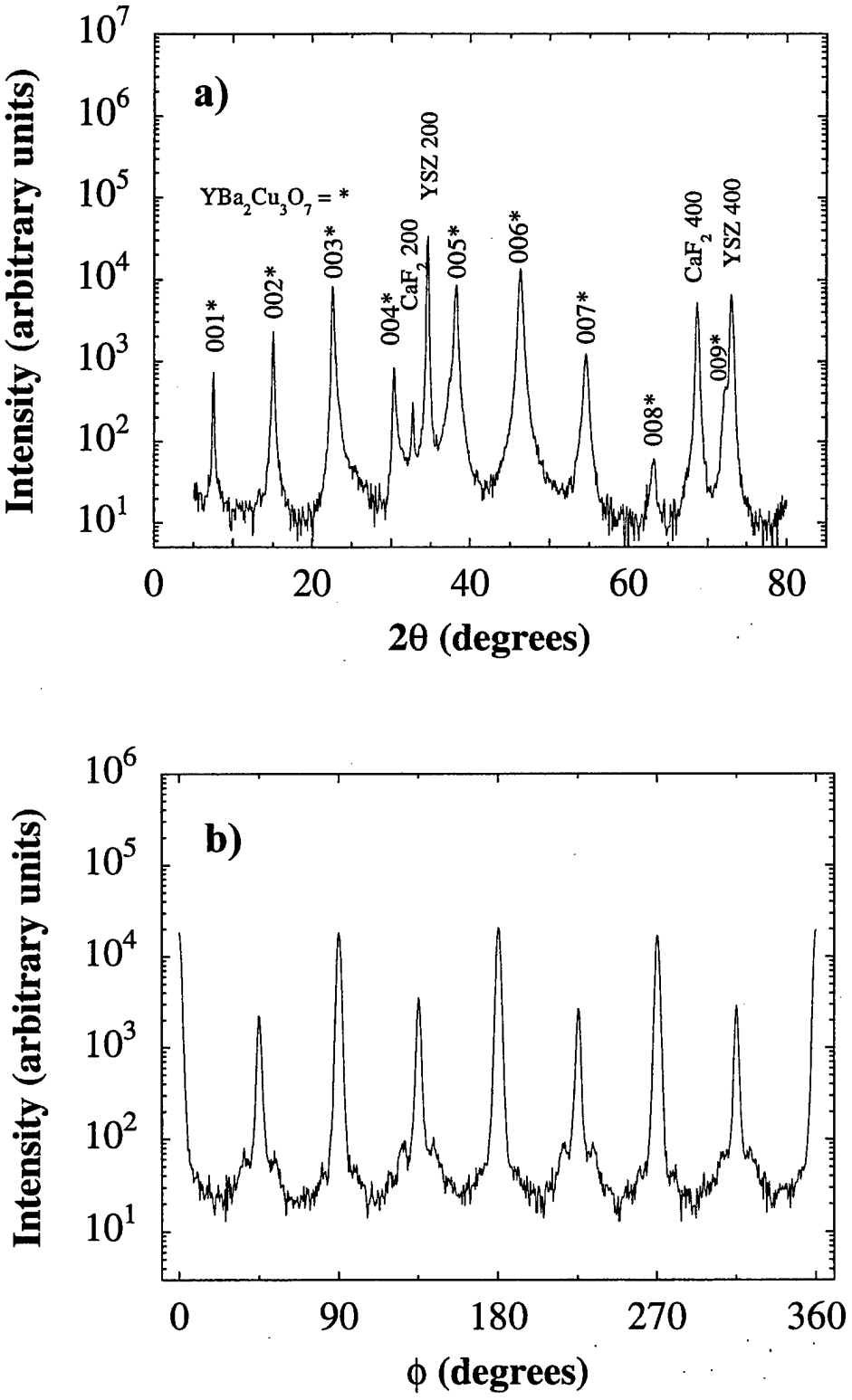

Figure 16. XRD patterns for a YBCO film grown at 785 °C on YSZ-buffered CaF_2(100): a) two theta scan, b) phi scan of the YBCO(103) peak.

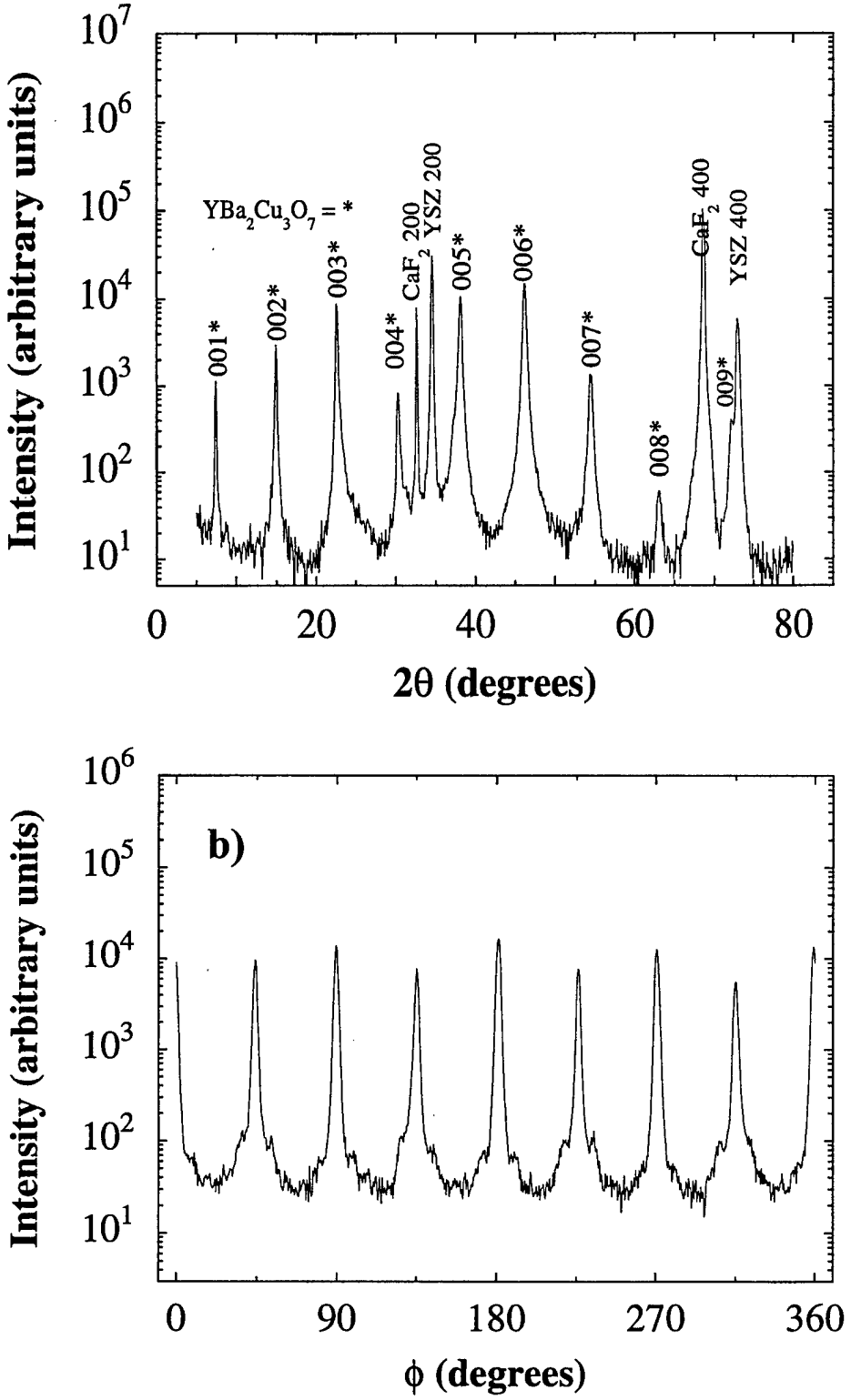

Figure 17. XRD patterns for a YBCO film grown at 810 °C on YSZ-buffered CaF_2(100): a) two-theta scan, b) phi scan of YBCO(103) peak.

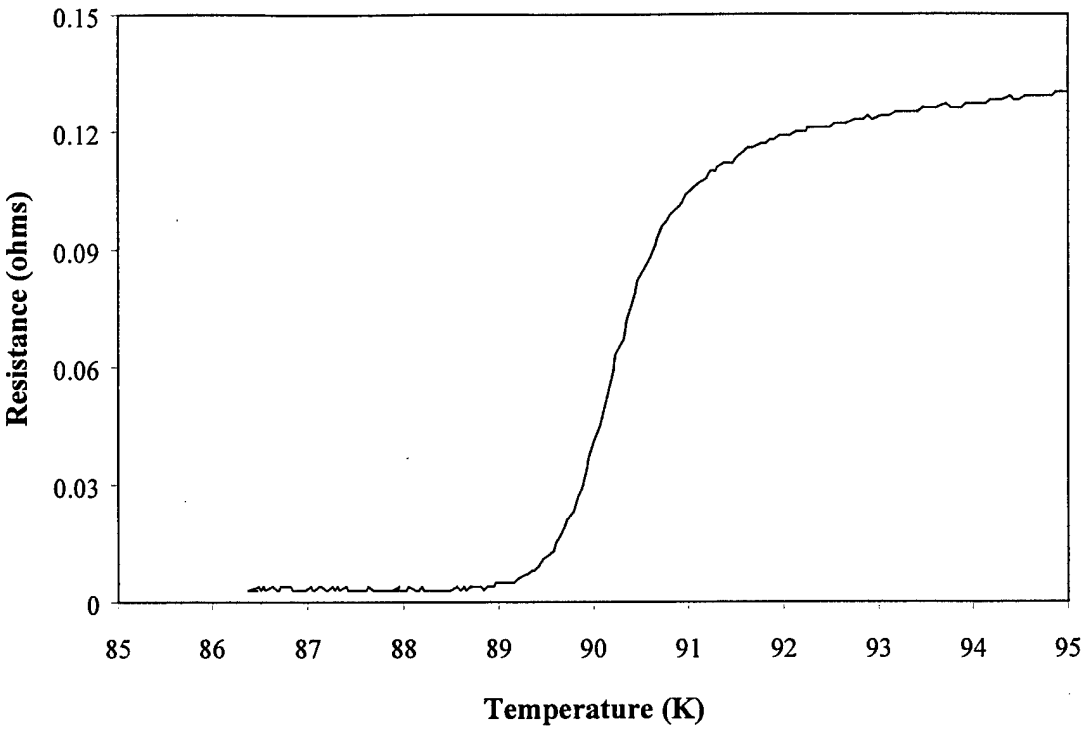

Figure 18. Resistance vs temperature for a YBCO film grown at 810 °C on YSZ-buffered CaF_2(100). A T_c of ~ 88.5 K (neglecting the baseline offset) is shown.

Table 3 summarizes the results of the YBCO films grown on buffered CaF_2(100) at various deposition temperatures. Based on the ω rocking curve measurements, the out of plane grain alignment improved with increasing growth temperature. We also observed T_c to increase with increasing growth temperature. However, although all films were c-axis oriented and epitaxial, XRD phi scans revealed that the films grown at higher temperatures consist of two domains, which precludes their use in devices. This twinning can be minimized either by nucleating the YBCO at 700 °C and continuing the deposition at a higher temperature or by using the double buffer (CeO_2/YSZ) layers.

Table 3. **Summary of film properties YBCO grown on buffered CaF_2 substrates.**

YBCO Deposition Temperature (C)	Buffer Layer(s)	ω (FWHM)	T_c (K)	Comments
700	YSZ	1.8°	...	Single Domain*
750	YSZ	1.3°	...	Some Twinning
750	YSZ	...	81	...
785	YSZ	0.95°	86.5	Two Domains
810	YSZ	0.82°	88.5	Two Domains
700, 780	YSZ	0.64°	...	Single Domain*
780	CeO_2/YSZ	0.55°	...	Single Domain*

* ≥ 99 %

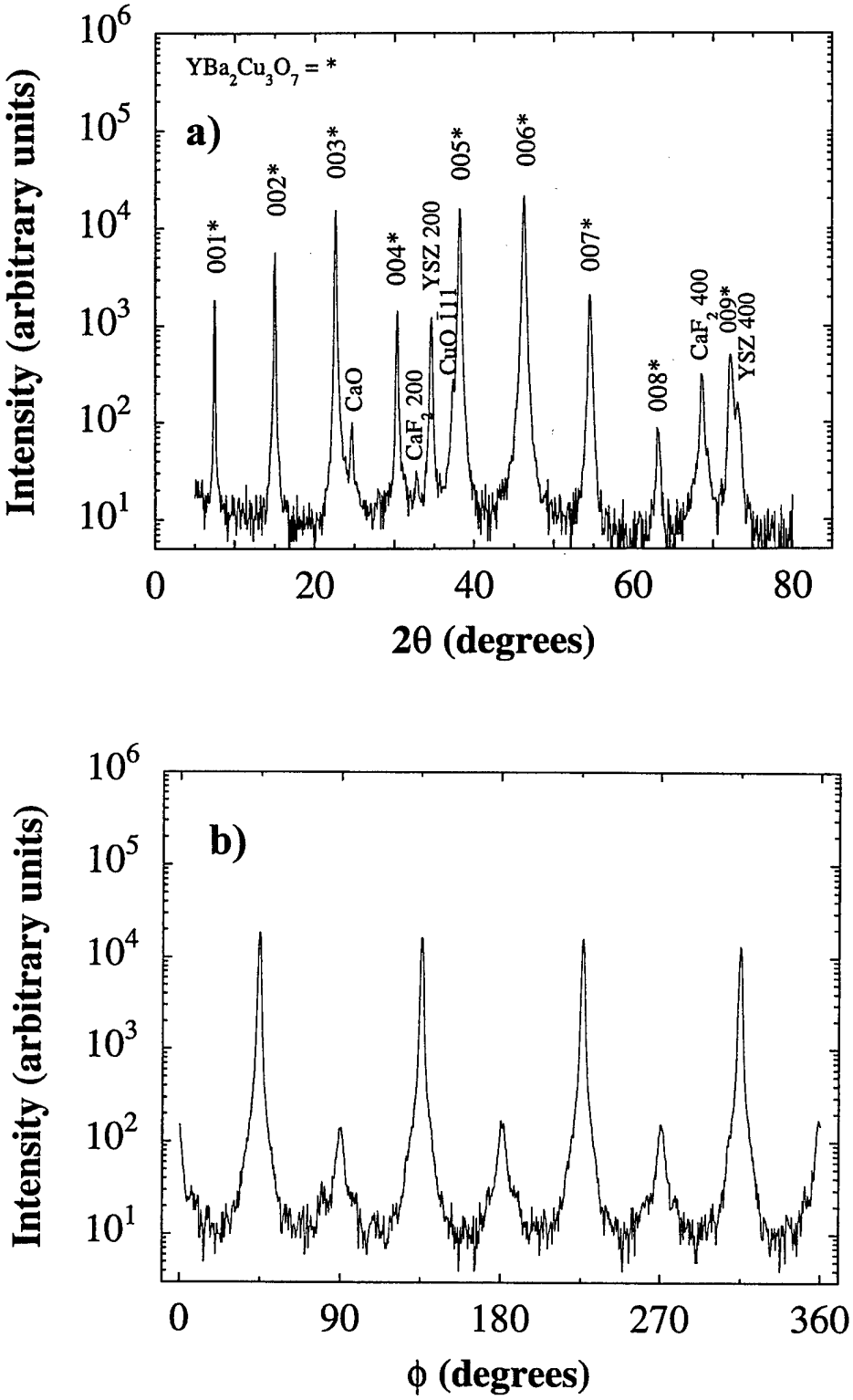

Figure 19. XRD patterns for a YBCO film, using a two-step growth temperature sequence, on YSZ-buffered CaF_2(100): a) two theta scan, b) phi scan of the YBCO(103) peak.

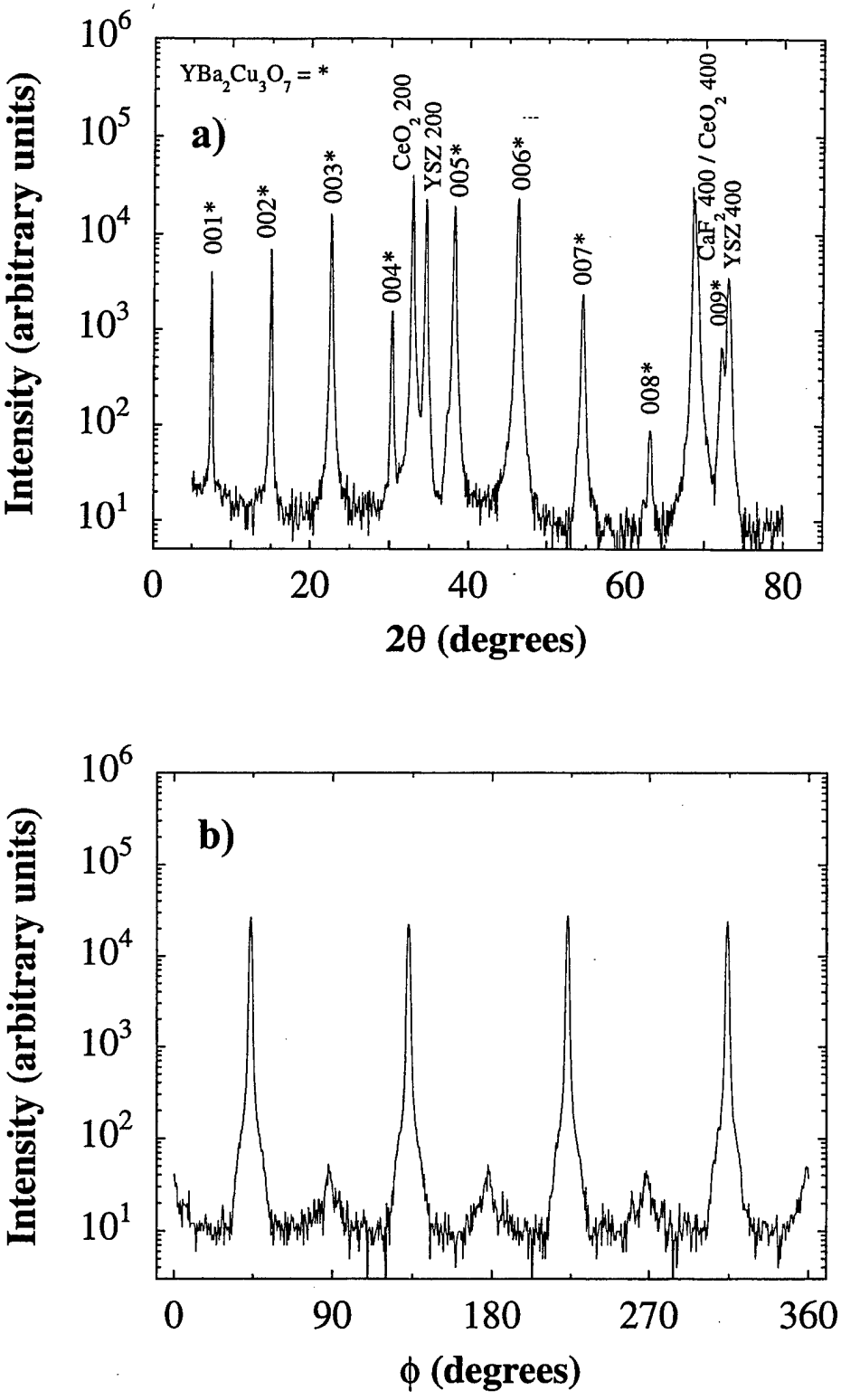

Figure 20. XRD patterns for a YBCO film grown at 785 °C on CeO_2/YSZ-buffered CaF_2(100): a) two-theta scan, b) phi scan of the YBCO(103) peak.

These results demonstrated that potentially high quality YBCO films could be grown on YSZ-buffered CaF_2(100) surfaces, particularly with further optimization of the deposition process. Our next step in this task was to deposit YBCO on CaF_2-buffered Si(100) with an intermediate YSZ layer. Initially, we purchased a CaF_2 target and several attempts to deposit CaF_2 films on Si(100) by PLD were made. The results were not encouraging in that the films were heavily laden with particles. One film was sent to Penn State for XRD analysis, however no evidence of CaF_2 was detected.

CaF_2 can be grown epitaxially on Si(111), Si(110) and Si(100) using traditional thermal evaporation techniques. Early work showed that the best films, in terms of crystallinity and morphology (smoothness), were grown on Si(111) substrates due to the fact that the (111) CaF_2 surface has the lowest free energy [24]. Films deposited on Si(100), although epitaxial, exhibited inferior crystalline quality and were too rough for any practical device applications. The surface roughness, a result of {111} faceting, was first observed by Fathauer and Schowalter [25] through reflective high energy electron diffraction (RHEED) experiments and later by Asano et.al. [24] using cross-sectional transmission electron microscopy. The cause of the faceting is believed to be due to the relatively low (111) surface free energy as compared to the (100) surface.

Dramatic improvements in both the crystallinity and morphology of CaF_2 films grown on Si(100) have been achieved by post-deposition thermal annealing. Pfeiffer et.al. [26] demonstrated improved structural, mechanical, chemical and electrical properties of MBE-grown CaF_2 films post-annealed (in a rapid thermal processing tool in an Ar background) at 1100 °C for periods of ~ 20 seconds. Microcracks were observed, however, that were suspected of being caused by differential thermal contraction during cooldown. More recent work by Asano et.al. [24] showed that significant improvements in film quality were obtained at annealing temperatures as low as 650 °C. The best films, however, were obtained by annealing at 900 °C. RBS ion-channeling measurements indicated that the crystalline quality of these films was comparable to bulk CaF_2. The group also compared CaF_2 films that were annealed *ex-situ* (where the sample was transferred to an annealing chamber after deposition) to films annealed *in-situ* (where the sample was heated in the growth chamber following deposition). Crack-free films were consistently obtained by the in-situ anneal while microcracks were typically observed in the ex-situ annealed films.

We therefore constructed a thermal evaporation system to deposit CaF_2 on Si(100). High purity CaF_2 powder is evaporated in a graphite crucible, heated by a tantalum ribbon crucible heater. The configuration provides a maximum deposition rate of 0.1 nm/sec and can be increased to higher rates by employing a larger crucible, if desired.

To optimize CaF_2 thin film growth, we primarily investigated the role of substrate temperature during deposition. Initially, single layer films of CaF_2 on Si(100) were deposited by thermal evaporation at substrate temperatures ranging from 550 °C to 750 °C and were sent to Penn State for x-ray diffraction (XRD) analysis. The results were somewhat inconclusive in that the two-theta scans showed no peaks other than those assignable to Si. However, further measurements by rocking did indicate the presence of a shoulder on the Si(400) peak for the film grown at 550 °C. This is not surprising since the lattice parameter for CaF_2 is only 0.6% larger than that of Si at room temperature. No shoulder, however, was observed for a film grown at 750 °C.

To enable more accurate assessment of film quality, it was decided that all samples sent out for XRD analysis hereafter would also include an additional layer of YSZ, which can be fully resolved from the Si – the opinion being that the structural quality of the YSZ would be dependent on the structural quality of the CaF_2. A new set of CaF_2 films on Si was grown at substrate temperatures ranging from 450 °C to 750 °C , each coated (by PLD) with ~ 100 nm of YSZ using our standard recipe for YSZ growth on Si. The

"best" film in this set of samples was grown at 550 °C. Films grown at 450 °C or at higher temperatures (≥ 625 °C) showed no XRD peaks assignable to YSZ and were classified as amorphous. For the CaF_2 film grown at 550 °C, the two-theta and phi scans, shown in Figure 21, indicate that the YSZ is epitaxial, although the phi scan peaks are quite broad (FWHM ~ 10°). Rocking curves also indicate that the crystalline quality is rather poor (FWHM = 4.5°).

In addition to XRD analysis, we also studied the morphology of the CaF_2 films (uncoated and coated with YSZ) by scanning electron microscopy (SEM). The surface of all films was found to be quite rough, consisting of triangular facets on order of 100 – 200 nm in size – too rough for device applications. These results are consistent with the results of others who observe (111) facets on the surface of epitaxial CaF_2 grown on Si(100) and may be due to the much lower free energy of the (111) surface as compared to the (100) surface of CaF_2 [24].

To reduce the surface roughness and improve crystalline quality, we investigated two approaches as prescribed by Asano et al. [24]. The first utilizes a two step growth method in which the CaF_2 film is nucleated at 550 °C and the majority of the film is grown at a higher temperature. We have observed dramatic improvements in film quality when the two step technique is employed. Our highest quality film using this technique was achieved by nucleating the first ~ 30 nm of CaF_2 at 550 °C followed by a ramp up to 675 °C for the remainder of the deposition (~ 150 nm). XRD analysis of the YSZ peaks indicates that the film is epitaxial, with a rocking curve FWHM = 1.2°. In addition, the width of the phi scan peaks is also much narrower (FWHM ~ 2.7°). Moreover, SEM analysis reveals a significant reduction in surface roughness.

In the second approach, the CaF_2 film was subjected to an *in-situ* rapid thermal anneal (RTA) immediately following deposition. The best film obtained by any of the techniques we have explored so far was grown at 550 °C for the entire deposition followed by a thermal anneal at 900 °C for 30 seconds. Figure 22 depicts the XRD two-theta and phi scan, demonstrating that the YSZ and, presumably, the CaF_2 layers are epitaxial. The presence of only the YSZ(200) and (400) peaks and the Si(400)/CaF_2(400) peak in the two-theta scan (Figure 22a) indicate that the YSZ and CaF_2 layers are well-oriented with respect to the substrate normal. Peaks spaced every 90° in the phi scan (Figure 22b) of the YSZ(311) peak establish in-plane epitaxy for the YSZ, and presumably the CaF_2. The FWHM of the phi peaks and omega rocking curves were determined to be ~ 2° and 1.0°, respectively, which is comparable to our YSZ films routinely grown on bare, single crystal Si. Also, SEM revealed that this was the smoothest film grown and no microcracks were observed.

Our work showed that epitaxial CaF_2 is achieved only when nucleation occurs in a narrow substrate temperature window centered around 550 °C, which is consistent with results of others. We also noted that substrate cleanliness played an important role in the epitaxial quality of the CaF_2 films. We found that CaF_2 films grown on silicon substrates that had been cleaned with organic solvents and spin-etched to remove the native oxide (which is our typical preparation technique for depositing YBCO/YSZ on bare Si) were not epitaxial. Epitaxy was only achieved when the Si was carefully cleaned using the traditional RCA process, followed by removal of the native oxide by spin-etching.

At this point we had established conditions for growing high quality YBCO on CaF_2(100) (with suitable buffer layers). We also had established deposition (substrate temperature) conditions for growing what we considered to be reasonable quality CaF_2 films on Si(100). Clearly, however, continued optimization of the deposition parameters was called for in order to achieve the highest quality CaF_2 (which we believed would be necessary to act as a compliant buffer layer). Parameters to be explored included, 1) substrate preparation, 2) deposition rate, and 3) substrate temperature, such as a combination of the two-

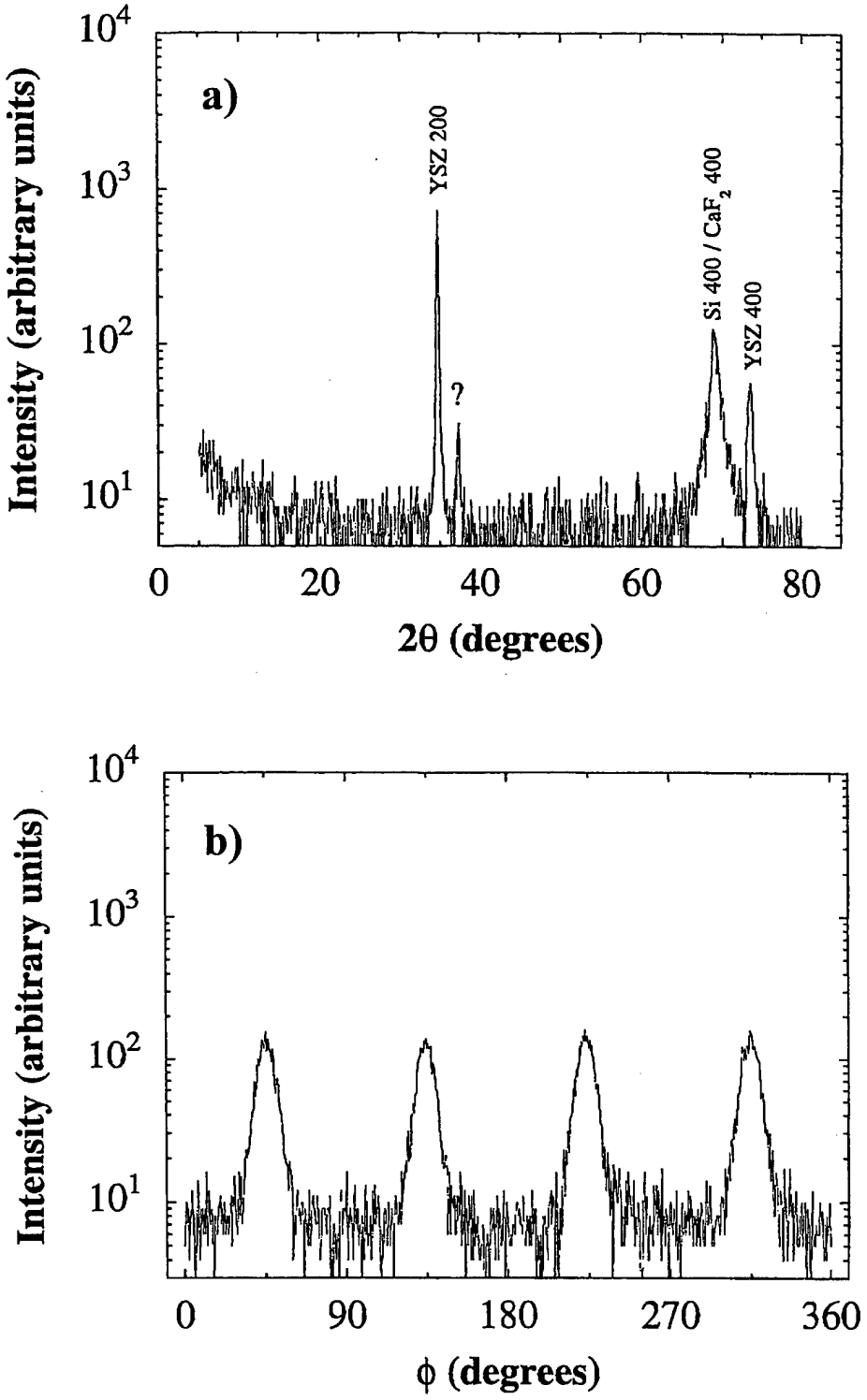

Figure 21. XRD patterns for a YSZ/CaF_2 filmstack grown at 550 °C on Si(100): a) two-theta scan, b) phi scan of the YSZ(311) peak. Because of the similar lattice parameters for CaF_2 and Si, the CaF_2 peak cannot be resolved from the Si peak. The CaF_2 film is assumed to be epitaxial since the YSZ overlayer is shown to be epitaxial.

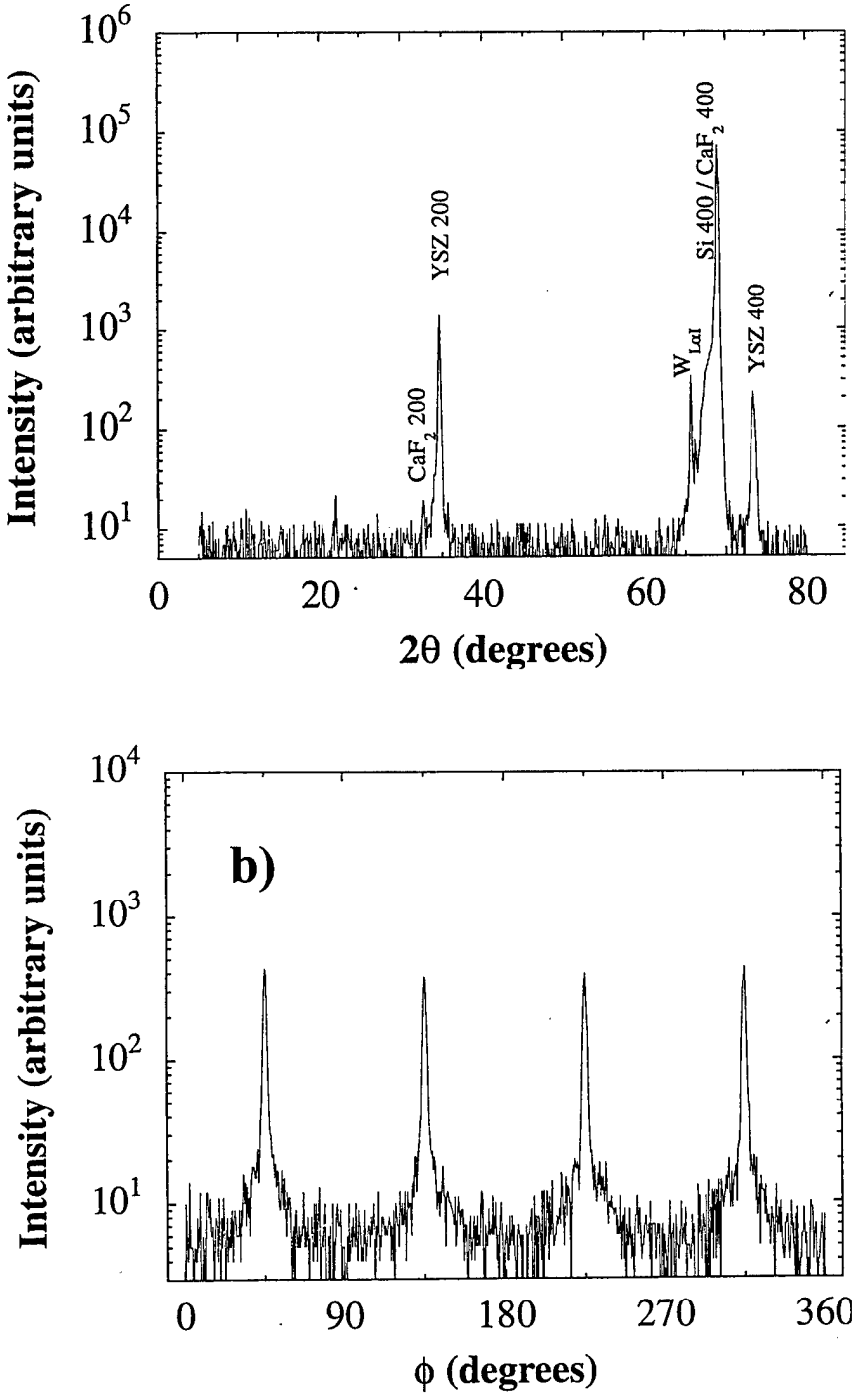

Figure 22. X-ray diffraction patterns for a YSZ/CaF_2 filmstack grown at 550 °C on Si(100), followed by an in-situ rapid thermal anneal: a) two-theta scan and, b) phi scan of the YSZ(311) peak. Peaks every 90° show in-plane epitaxy of the YSZ overlayer. This implies that the CaF_2 underlayer is epitaxial as well.

step method and rapid thermal anneal. However, we also felt that, in parallel, we should begin growing YBCO on the CaF_2-buffered Si we were, at the time, producing.

In a limited number of attempts, we were able to deposit superconducting YBCO on CaF_2-buffered Si. Figure 23 presents XRD data obtained for a ~ 120 nm thick YBCO film grown (substrate temperature ~ 750 °C) on CaF_2-coated Si, with an intermediate YSZ layer. The film is epitaxial, as evidenced in the phi scan (Figure 23b), however, there is obvious in-plane twinning, similar to what we observed for YBCO grown on the YSZ-buffered single crystal CaF_2 substrates, at higher temperatures. Again, the in-plane twinning was virtually eliminated by employing the double buffer, CeO_2/YSZ, as shown in Figure 24, for an epitaxial filmstack consisting of YBCO/CeO_2/YSZ/CaF_2/Si(100) (YBCO thickness ~ 150 nm). We also observed in both samples that, although the majority of the films were c-axis oriented, there was a minor but significant fraction of a-axis oriented grains, much more so than with the films grown on the CaF_2 substrates. The reason is not clear, however we suspect that substrate temperature may have been a factor.

Figure 25 presents the resistance vs temperature for the single domain YBCO/CeO_2/YSZ/CaF_2/Si(100) film. As shown, the film displayed a T_c ~ 88.5 K. The transition actually is fairly sharp, however there is a noticeable tail, consistent with film microcracking, which was confirmed by SEM analysis.

In this limited number of attempts, we did not successfully grow crack-free YBCO, thicker than 70 nm, on CaF_2 buffered Si. At this point, we believed that either or both of the following two reasons were possible. First, as mentioned above, we felt that the best conditions for CaF_2 growth had not been established, and significant improvements to the film quality were expected with further optimization of the deposition conditions. Our opinion was that very high quality CaF_2 was necessary to obtain stress relief in the YBCO overlayers. Second, there was evidence that the CaF_2 was being at least partially oxidized during the YBCO deposition. Note, in Figures 23a and 24a, the presence of a CaO(200) peak at two-theta ~ 37°, suggesting a reaction at the CaF_2/YSZ interface to form a textured CaO interlayer. We even observe some CaO formation in the poor quality YSZ/CaF_2 sample shown in Figure 21a (labelled as ?). It is unclear whether CaO was forming in the YBCO samples grown on the CaF_2 substrates, however, upon close examination of the XRD two-theta scans (Figures 15 – 17, 19,20), we observe a shoulder on the YBCO(005) peak at the angle expected for the CaO(200) peak, suggesting that the CaF_2 substrate was also being oxidized. The CaO may impede the movement of dislocations in the CaF_2, thus rendering the CaF_2 useless for stress relief. This is consistent with observations by others, as described earlier, who have shown that CaF_2 films which are subjected to an ex-situ rapid thermal anneal (i.e., the films are briefly exposed to ambient oxygen) develop microcracks upon cooling.

Based on these data, we believed that continued optimization of the CaF_2 film growth was needed, but we also believed that it would be necessary to protect the CaF_2 layer from oxidation during the YBCO/YSZ growth step. We suspect that oxygen was diffusing through the YSZ (being a good oxygen conductor), particularly during YBCO growth, to form the CaO. (A thin amorphous SiO_2 layer is known to form at the YSZ/Si interface during growth of YBCO/YSZ on Si [27].) Clearly, an oxygen diffusion barrier would need to be deposited on the CaF_2 in-situ (without breaking vacuum) before transfer to the YBCO deposition system. Two options were available which could be explored. First, the YSZ layer could be replaced by a less oxygen conductive film, such as MgO or $SrTiO_3$ [28], however, this would require substantial work to verify if the CaF_2 would support epitaxial growth of MgO or $SrTiO_3$. In particular, there was concern regarding possible chemical reactions to form MgF_2 or SrF_2.

A more attractive approach would be to add a diffusion barrier between the CaF_2 and YSZ. The obvious candidate was, of course, Si. Previous work [29] demonstrated that Si could be grown epitaxially on CaF_2 and we have extensive experience in high quality growth of YBCO on buffered Si. In addition, a

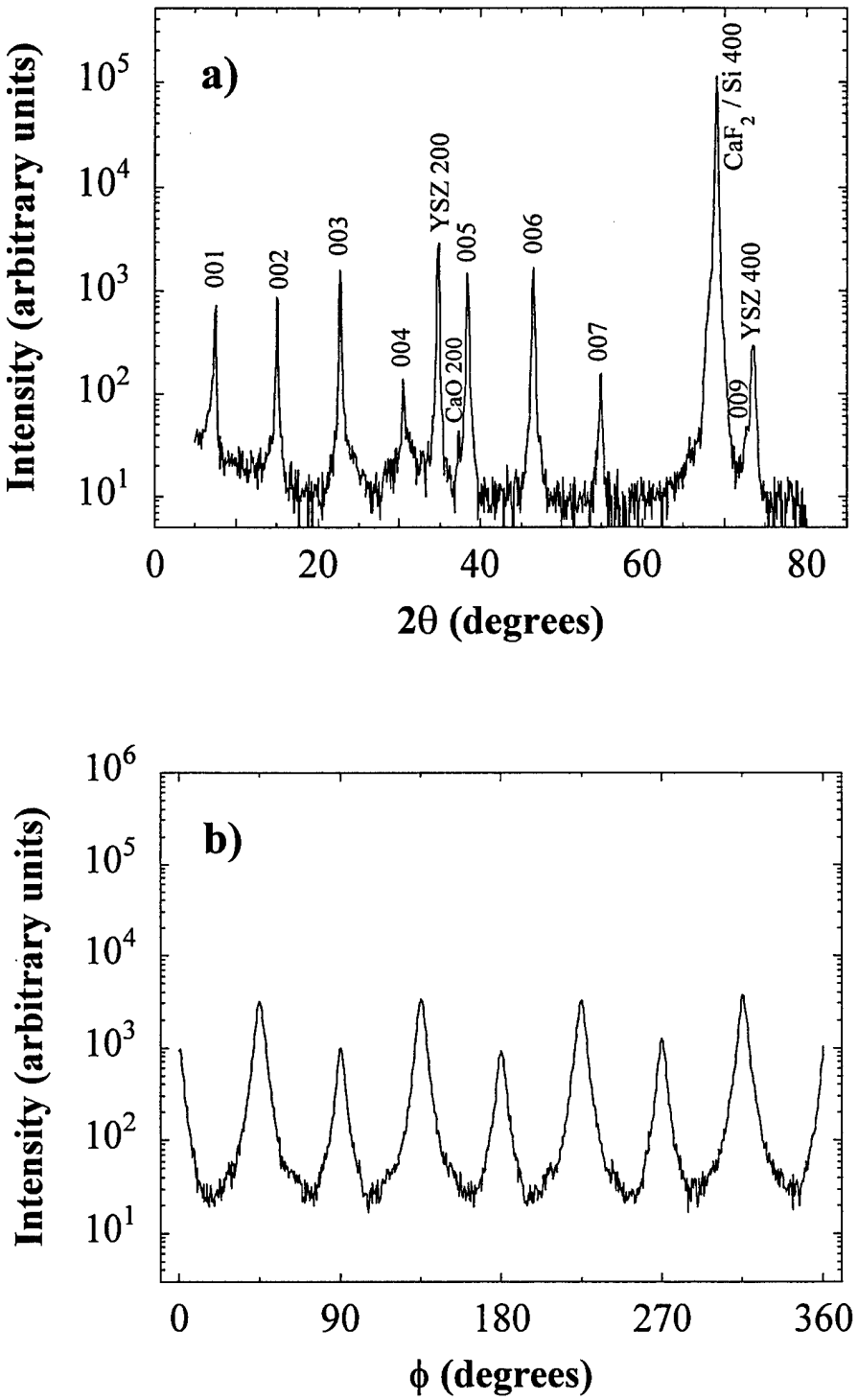

Figure 23. XRD patterns for a YBCO/YSZ/CaF_2 filmstack grown on Si(100): a) two-theta scan and, b) phi scan of the YBCO(103) peak revealing that the film is epitaxial but consists of a mixture of two domains.

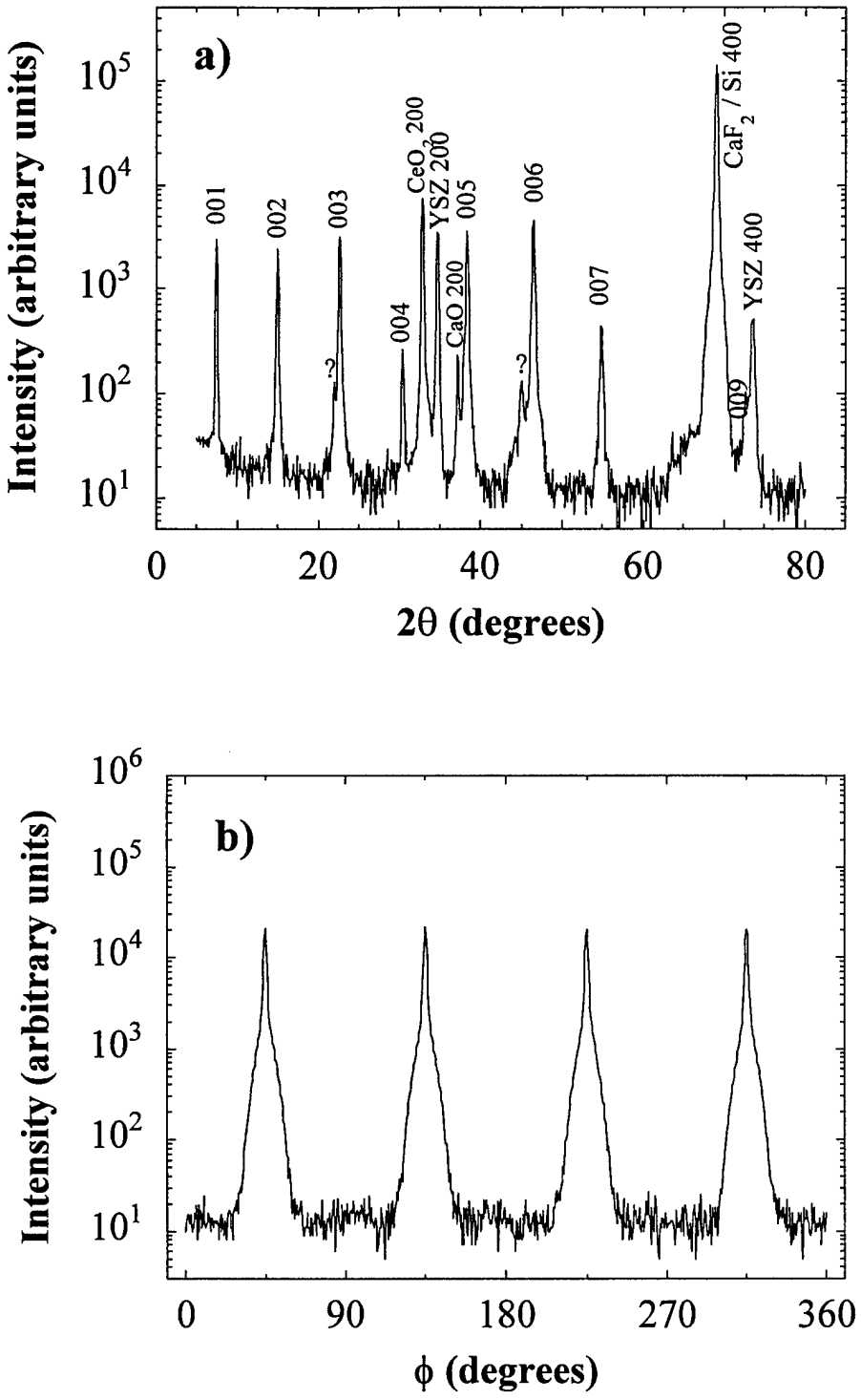

Figure 24. XRD patterns for a YBCO/CeO_2/YSZ/CaF_2 filmstack grown on Si(100): a) two-theta scan and b) phi scan of the YBCO(103) peak. The YBCO is shown to be epitaxial and single domain.

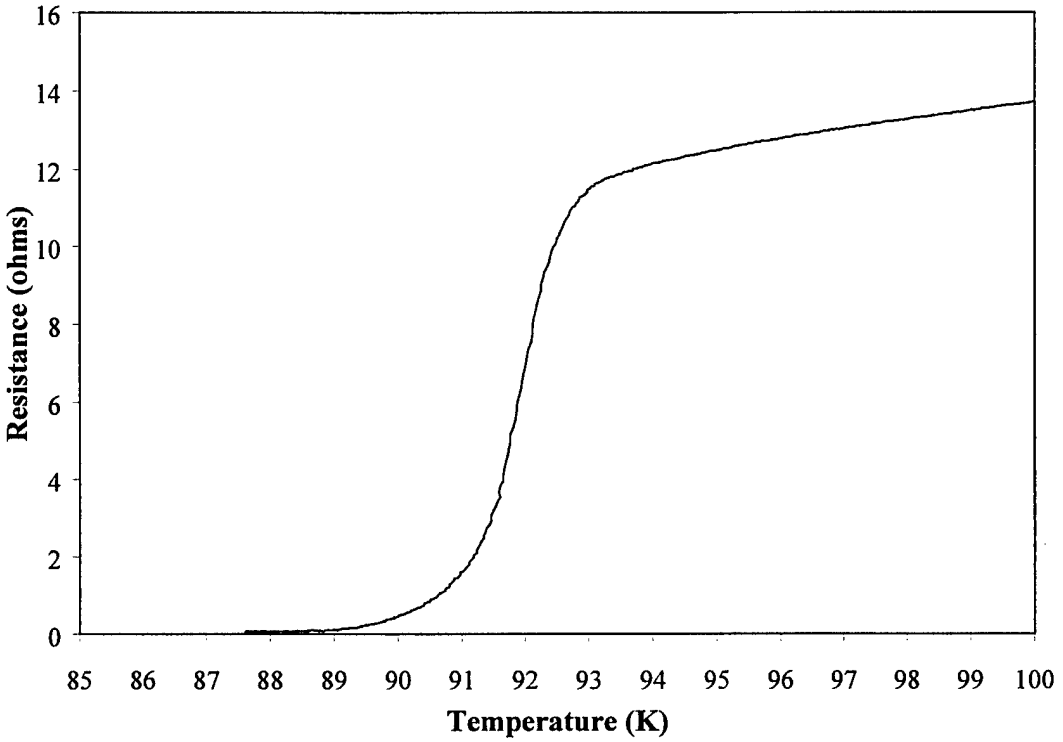

Figure 25. Resistance vs Temperature for a YBCO/CeO_2/YSZ/CaF_2/Si(100) film showing a Tc ~ 88.5 K. The tail in the transition suggests microcracks in the YBCO, which was confirmed by SEM.

SiH_4/H_2 gas delivery system was available in our laboratory for chemical vapor deposition (CVD) of Si. A simple modification to our evaporation system would enable us to deposit CaF_2 followed by Si on the Si substrates. When completed, the sample would be removed from the system, H-terminated by our spin-etch process and inserted in the PLD system for YBCO/(CeO_2)/YSZ growth. Again, however, we were unable to investigate this promising solution because of the untimely equipment and personnel problems at SUNY (see Task 5 for details).

Task 4: Film Characterization and Stress Analysis - To measure structure, morphology, stress and electrical properties of $YBa_2Cu_3O_7$ films and devices.

The goal of this task was simply to characterize the array of HTS films and buffer layers investigated in Tasks 1-3, as well as the junction-based devices fabricated Task 5. Extensive characterization of the thin film materials prepared at AFR in this project has been discussed in detail in Tasks 1-3.

Task 5: Demonstration Circuits - To demonstrate working HTS electronic circuits on silicon, sapphire, and compliant substrates.

The goal of this task was to demonstrate HTS junction-based devices on silicon and other more practical high speed substrates of commercial interest. The plan was to start with relatively simple structures, and work our way towards more complex RSFQ devices and circuits. Initially, we would fabricate those devices that could be constructed from a single superconducting layer, such as:

- Single junctions and SQUIDs
- Josephson transmission lines
- DC/SFQ converter
- SFQ/DC converter
- T Flip-Flop
- RS Flip-Flop

As the ability to fabricate multilayered elements became possible through Task 3, we would explore fabrication of RSFQ gates with electrically insulated (passive) groundplanes as well as gates exploiting active connections between wiring and groundplane layers.

Unfortunately, around the time that AFR started sending to SUNY high quality YBCO films on Si (prepared in Task 1), SUNY experienced equipment problems, specifically with the e-beam writing apparatus. SUNY was unable to fabricate junctions on our samples because of computer hardware and software problems with the Philips CM-12 electron microscope used in the writing process – the original Phillips computer with the writing programs had died and there were hardware and software compatibility problems with the replacement Power Mac PC. In addition, SUNY's senior scientist in charge of the experimental junction work, Dr. Sergey Tolpygo, transferred to another department, which only exacerbated the situation. For several months, SUNY attempted to restore the equipment and personnel problems but the situation was never resolved during the remainder of the program. During this time period, we continued our work in Tasks 2 and 3, but when it became evident that SUNY's situation would not be resolved, the program was halted.

Task 6: Advanced Demonstration Circuits - To design, fabricate, and test circuits comprised of multiple RSFQ elements and passive rf structures.

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